UNICMICRO 广芯微电子

# UM3500F

## USB Type-C Port Controller with DPDM CHG Detection

### Description

UM3500F is a USB standard compliant Type-C Port Controller (TCPC) that enables a USB Type-C port with the Configuration Channel (CC) logic needed for USB Type-C ecosystems. It integrates the essential physical layer of the USB power delivery (PD) protocol to allow up to 100W of power.
UM3500F can be accessed by a standard compliant Type-C Port Manager (TCPM) which flexibly resides in external MCU/EC/AP etc. through standard I2C interface. Under control of the TCPM, UM3500F uses the CC pins to determine port attach/detach, cable orientation, role detection, and port control for USB Type-C function. The UM3500F can be configured as SRC, SNK or DRP, depending on the application. The UM3500F implements VBUS detection and discharge for a compliant USB Type-C port. The UM3500F integrates 100mW switch to provide VCONN power for E-mark cable and provides VCONN discharge function. The UM3500F also supports USB Type-C optional features such as audio and debug accessory mode.

Additionally, the UM3500F integrates USB charge detection interface for QC2.0/3.0 and FCP, SCP. The UM3500F monitors USB DP/DM and automatically adjusts the output voltage depending on different powered device. If the powered device doesn't support USB PD protocol, the UM3500F can support other protocol as mentioned above.

The UM3500F is available in UTQFN-24L, TQFN-16, *TQFN-20 (TBD)* packages.

### Features

USB PD and Type-C:
- Supports USB Type-C™ 1.2 and TCPCI 1.2
  - Support Type-C attach/Detach, Orientation detection
  - Support Type-C DRP for Power Sourcing and Sinking
  - Support Dead Battery Support (Optional)
  - 100mW VCONN Power (20mA)
- Data Chunked and PPS Support
- VBUS and VCONN Discharge Function
- Fast Role Swap Support
- Cooperate with TCPM for full function PD system

DP/DM CHG Detect (for Source Only):
- Support QC 2.0/3.0, Voltage from 3.6V to 12V for Class A and 20V for Class B
- Support FCP & SCP
- Automatically Selects FCP/SCP and QC2.0/3.0 Protocols
- Supports USB DCP Applying 2.7V on DP and DM
- Supports USB DCP Shorting DP and DM per USB BC1.2

Others:
- Control of External N-CH MOSFETs for Source and Sink Power Path
- Low side CSA
- Fault pin Alarm for VBUS OVP, CC or DP/DM Short to VBUS
- User Defined I/O x 3 pins
- Low Current Consumption (< 30uA)

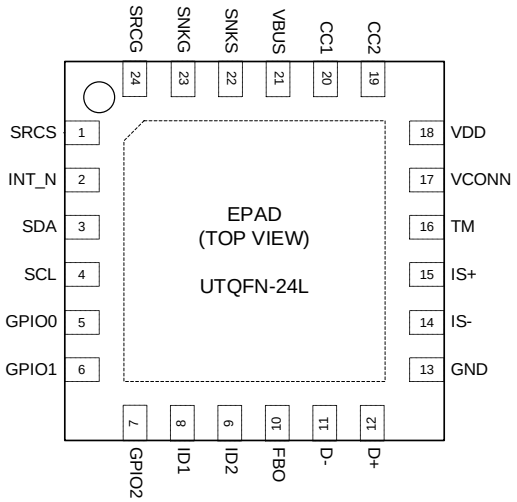
### Applications

- Charge accessories for Power Adapter, Power Banks, etc.
- Type-C Dongle with Alternate function
- Portable Device

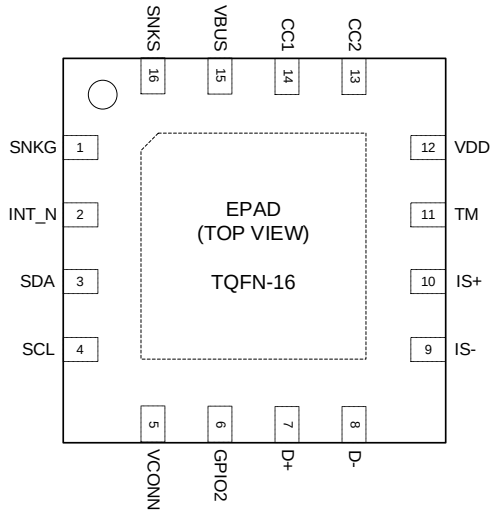
# 1 Pin Information

## 1.1 Pin Assignments

**UTQFN-24L (Exposed Pad, 4mm x 4mm)**




**TQFN-16(Exposed Pad, 4mm x 4mm)**




## 1.2 Pin Description

| Pin Name | Pin No. (UTQFN-24L) | Pin No. (TQFN-16) | Pin Function |
|---|---|---|---|
| SRCS | 1 | - | NMOS source note control (as source). |
| INT_N | 2 | 2 | Open drain output. Asserted low to indicate status change occurred. Requires an external pull-up resistor. |
| SDA | 3 | 3 | I2C communication data signal. Requires an external pull-up resistor. |
| SCL | 4 | 4 | I2C communication clock signal. Requires an external pull-up resistor. |

| | | | |
|---|---|---|---|
| GPIO 0~2 | 5,6,7 | 6 | Programable digital input/ouput pin. The GPIO 2 also can be configured as fault pin. |
| ID1 & 2 | 8,9 | | The I2C slave Address selection pins. |
| FBO | 10 | | Feedback output pin. Current sink/source FB node. |
| DM | 11 | 8 | USB DM for USB Charger detection |
| DP | 12 | 7 | USB DP for USB Charger Detection |
| GND | 13 | - | Ground. |
| IS− | 14 | 9 | Negative input of a current sense amplifier. Connect to the current sense resistor on the VBUS power path. |
| IS+ | 15 | 10 | Positive input of a current sense amplifier. Connect to the current sense resistor on the VBUS power path. This pin could be opened or connected to ground if user want to neglect the current of VBUS power path. |
| TM | 16 | 11 | External thermal sensor connection node (NTC). |
| VCONN | 17 | 5 | VCONN range from 2.7V to 5.5V. VCONN voltage should be at a valid stable value before TCPM turns on the VCONN switch. |
| VDD | 18 | 12 | 2.7V to 5.5V positive supply voltage. |
| CC2 | 19 | 13 | Type-C configuration channel signal 2. |
| CC1 | 20 | 14 | Type-C configuration channel signal 1. |
| VBUS | 21 | 15 | VBUS voltage detection. |
| SNKS | 22 | 16 | NMOS source note control (as sink). |
| SNKG | 23 | 1 | NMOS gate note control (as sink). |
| SRCG | 24 | - | NMOS gate note control (as source). |

# 2 Typical Application

## 2.1 Source Only – Dual Type-C Port Application

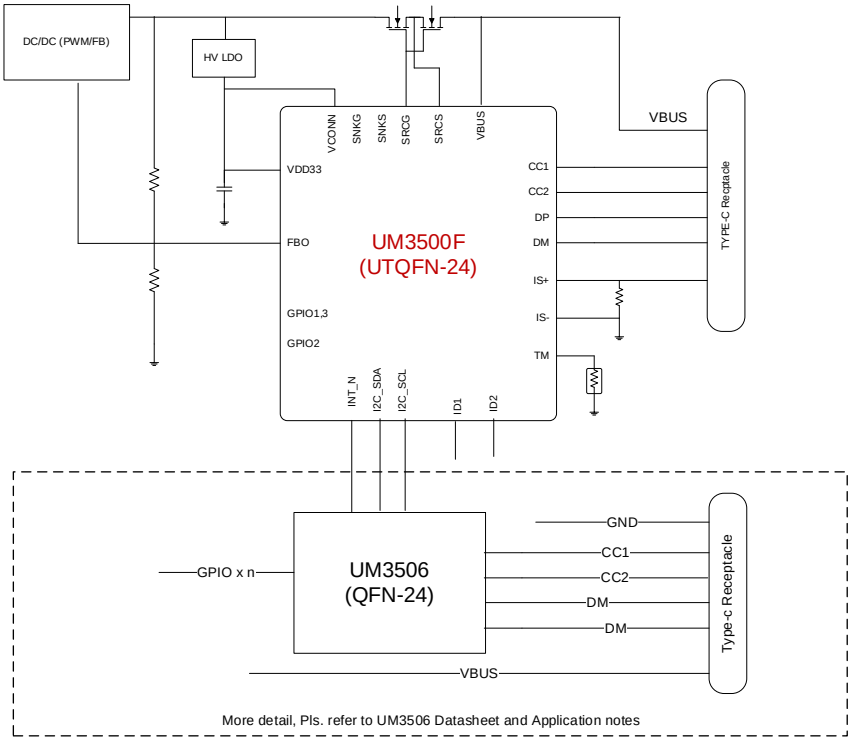



Figure 2-1 SRC Only for Dual-Port Application

## 2.2 DRP - Dual Type-C Port Application

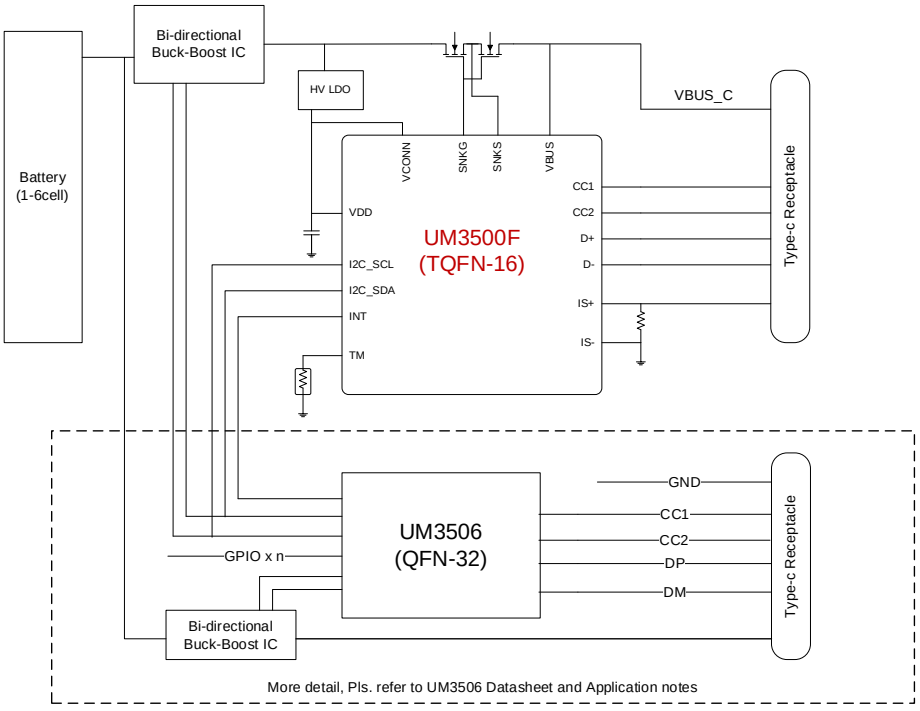



Figure 2-2 DRP for Dual-Port Application

## 2.3 DRP – n * Type-C Port Application

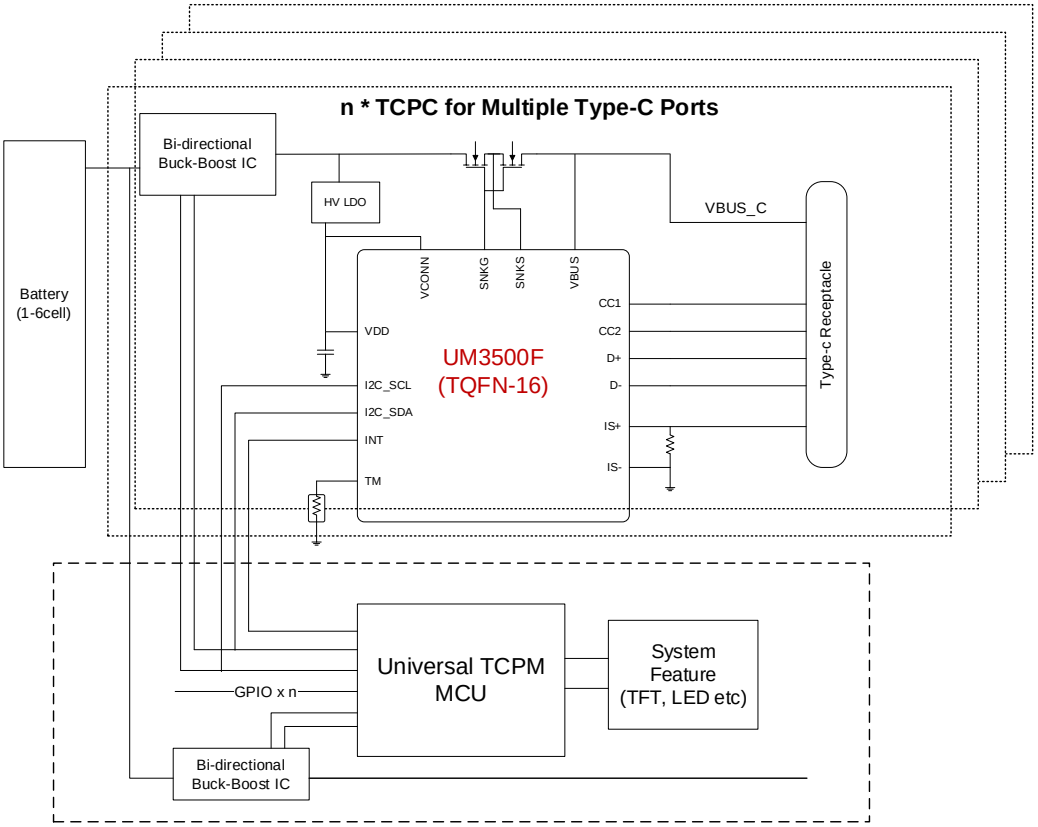



Figure 2-3 DRP for n-Port with TCPM Application

# 3 Functional Description

## 3.1 Functional Block Diagram

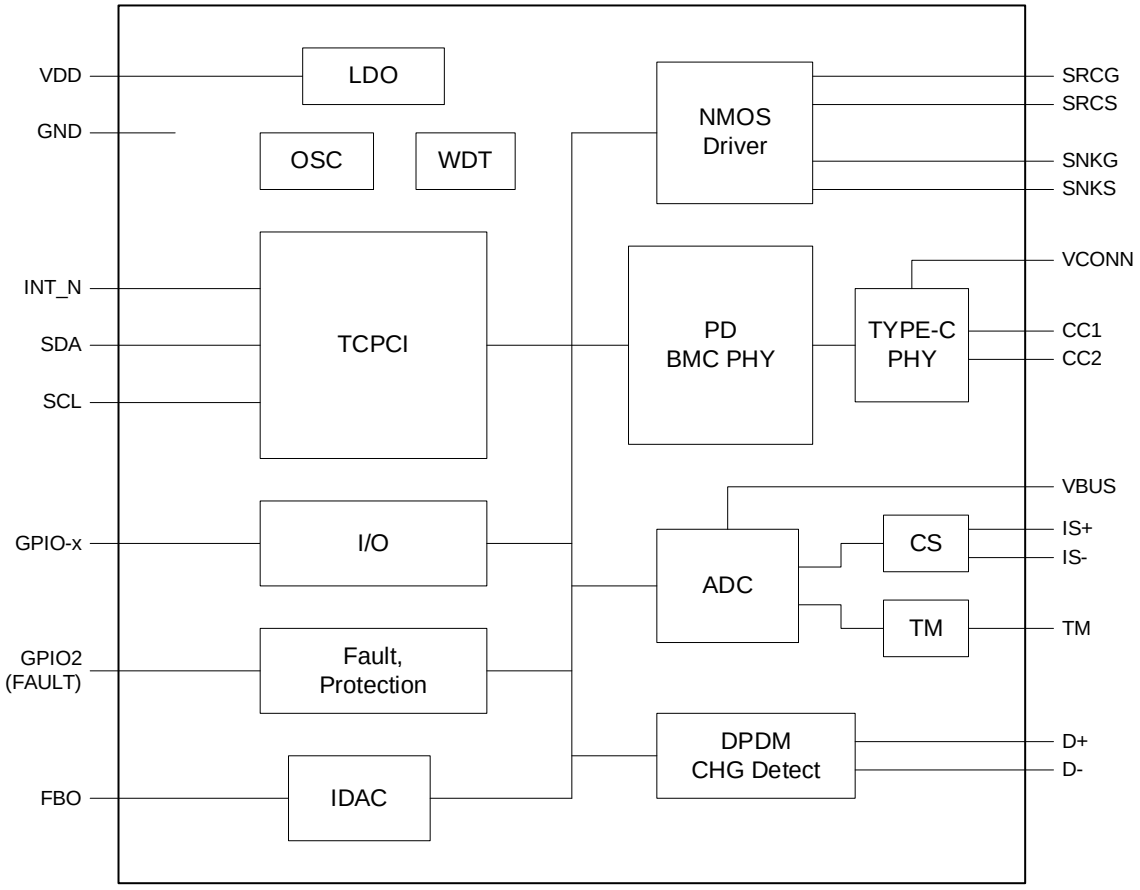



Figure 3-1 UM3500F Block Diagram

## 3.2 Function Description

**Slave Address Selection**

UM3500F supports four kinds of slave addresses, which is selected by TCPM. The default slave address of UM3500F is 0x60 and it could be changed by ID1 and ID2 pins through pull-high/low. Pls. refer to the following Slave Address.

- ID1 = 0, ID2 = 0; Slave Address is 0x60;
- ID1 = 0, ID2 = 1; Slave Address is 0x62;
- ID1 = 1, ID2 = 0; Slave Address is 0x64;
- ID1 = 1, ID2 = 1; Slave Address is 0x66;

**Dead Battery Function (for DRP)**

UM3500F could be applied to the power bank system due to the input voltage of UM3500F ranges from 2.7V to 5.5V. Moreover, when the battery is dead, UM3500F will automatically change the supplied power from input pin to VBUS pin and enable the NMOS_SNK driver. Please refer to the register 0xAC for setting the dead battery function.

**Overvoltage Protection**

UM3500F supports overvoltage protection of VBUS, CC1, CC2, DP and DM pin. The GPIO 2 (fault pin) will be pulled high when one of these pins is suffered from the high voltage. TCPM monitors the GPIO 2 (fault pin) and the abnormal information is therefore caught immediately. Additionally, the setting of OVP protection is assigned to the vendor define registers.

**Temperature Measurement**

UM3500F provides the TM pin connected to the NTC thermistor. The TM pin could source current and return the voltage on NTC thermistor to the register of UM3500F. Therefore, TCPM could access the voltage on NTC thermistor from the register of UM3500F and the temperature could be obtained by simple calculation. Please refer to the register 0xC0[6:5] and 0xC4.

**VBUS Control**

The UM3500F is a controller so that it must be combined with power stage. The FBO pin of UM3500F must be connected to the feedback node of power stage. The VBUS control of UM3500F is implemented by sourcing/sinking current from FBO pin. Please refer to the register 0xD0~0xD2 for detail information.

**Current Measurement**

UM3500F could monitor the current flowing from IS+ pin to IS− pin (for source role only). The current information is returned to register 0xC3. However, UM3500F do not support the over current protection. If the over current protection is needed, it must be implemented by power stage or other protection circuit.

**VCONN Over Temperature Protection**

VCONN switch is the only probably heating point in UM3500F due to the current limit of the VCONN switch is up to 40mA. When the temperature of the VCONN switch is higher than the 160°C the VCONN switch will be automatically turned off until the temperature decreases to 130°C.

**DPDM CHG Detection**

UM3500F supports QC 2.0/3.0/FCP and SCP protocol on the DP/DM data line. The related registers are assigned to the vendor define registers. These registers are public for user and could be managed by TCPM. When the UM3500F is configured as QC 2.0/3.0/FCP mode, both DP and DM pin are applied to 2.7V. If sink device has the function of QC 2.0/3.0/FCP, DP pin will be forced between 0.325V and 2V. In the meanwhile, DP pin will be automatically connected to DM pin by UM3500F and this process is called the short mode for USB BC1.2 specification. If DP is continuously applied to the voltage between 0.325V and 2V for 1.25 seconds, the UM3500F will enter QC 2.0/3.0/FCP operation mode. The QC 2.0/3.0 could be classed as the following.

- DP = 0.6V, DM = 0.6V; Output Voltage is 12V
- DP = 3.3V, DM = 0.6V; Output Voltage is 9V
- DP = 0.6V, DM = 3.3V; Output Voltage is Continuous mode
- DP = 0.6V, DM = High-Z; Output Voltage is Default 5V

When the voltage of DP pin and DM pin simultaneously satisfy these two inequalities VDAT(REF)< DP <VSEL_REF and D−> VSEL_REF, the UM3500F would enter continuous mode.
In the continuous mode, each voltage pulse on DP pin generated by sink device is between 1V and 3V. In the meanwhile, the high level of pulse should be kept at least 200us (default). If the specified conditions are satisfied, the FBO pin will sink 2uA (default) per pulse. The maximum sink current is 150uA for output voltage 20V.
In the continuous mode, each voltage pulse on DM pin generated by sink device is between 3V and 1V. At the same time, the low level of pulse should be kept at least 200us (default). If the specified conditions are satisfied, the FBO pin will source 2uA (default) per pulse. The maximum source current is 14uA for output voltage 3.6V. If the sink device doesn't support QC 2.0/3.0, the UM3500F will remain default output voltage 5V for safe operation. On the other hand, when USB cable is removed, the voltage of DP pin is therefore lower than VDAT(REF) and the output default voltage 5V is also applied.

**MTP Register table**

MTP function in UM3500F indicates thirty-two registers. Each page consists of four registers. Then, each chip includes eight pages. The Reg.0x98~Reg.0x9A are used to operate the MTP registers. The definition of MTP register could be refer to following table. However, both page 0 and page 1 are reserved by vendor.

| Chip | Page | Register Name | Register Address | MTP Address |
|---|---|---|---|---|
| | 0 | Reserved | 0xA0 | 0x00 |
| | | Reserved | 0xA1 | 0x01 |
| | | Reserved | 0xA2 | 0x02 |
| | | Reserved | 0xA3 | 0x03 |
| | 1 | QC_PROTOCOL_CONTROL_BYTE_0 | 0x9C | 0x04 |
| | | QC_PROTOCOL_CONTROL_BYTE_1 | 0x9D | 0x05 |
| | | Reserved | 0x9E | 0x06 |

| | | | | |
|---|---|---|---|---|
| 0 | | Reserved | 0x9F | 0x07 |
| | 2 | Reserved | 0xA4 | 0x08 |
| | | Reserved | 0xA5 | 0x09 |
| | | Reserved | 0xA6 | 0x0A |
| | | Reserved | 0xA7 | 0x0B |
| | 3 | Reserved | 0xA8 | 0x0C |
| | | Reserved | 0xA9 | 0x0D |
| | | Reserved | 0xAA | 0x0E |
| | | Reserved | 0xAB | 0x0F |
| | 4 | DEAD_BATTERY_VOLTAGE_SELECTION | 0xAC | 0x10 |
| | | Reserved | 0xAD | 0x11 |
| | | Reserved | 0xAE | 0x12 |
| | | FACTORY_ID | 0xAF | 0x13 |
| | 5 | VENDOR_ID_L | 0x00 | 0x14 |
| | | VENDOR_ID_H | 0x01 | 0x15 |
| | | USBTYPEC_REV_L | 0x06 | 0x16 |
| | | USBTYPEC_REV_H | 0x07 | 0x17 |
| | 6 | DEVICE_ID_L | 0x04 | 0x18 |
| | | DEVICE_ID_H | 0x05 | 0x19 |
| | | DEVICE_CAPABILITIES_1_L | 0x24 | 0x1A |
| | | DEVICE_CAPABILITIES_1_H | 0x25 | 0x1B |
| | 7 | DEVICE_CAPABILITIES_2_L | 0x26 | 0x1C |
| | | DEVICE_CAPABILITIES_2_H | 0x27 | 0x1D |
| | | STANDARD_INPUT_CAPABILITIES | 0x28 | 0x1E |
| | | STANDARD_OUTPUT_CAPABILITIES | 0x29 | 0x1F |

# 4 Electrical Characteristics

## 4.1 Absolute Maximum Ratings

| Parameter | Rating | Unit |
|---|---|---|
| Supply voltage VDD | -0.3 ~ +6.5 | V |
| VCONN | -0.3 ~ +6.5 | V |
| INT_N, SDA, SCL | -0.3 ~ +24 | V |
| CC1, CC2, VBUS | -0.3 ~ +24 | V |
| DP, DM | -0.3 ~ +12 | V |
| SRCS, SNKS, SRCG, SNKG | -0.3 ~ +35 | V |
| GPIO 0~4 | -0.3 ~ +6.5 | V |
| IS+, IS−, FBO, TM | -0.3 ~ +6.5 | V |
| Maximum junction temperature (TJ) | +150 | °C |
| Storage temperature (TStg) | 65 ~ +150 | °C |
| Lead temperature (Soldering, 10sec.) | +260 | °C |
| Power dissipation @TA=25℃, (PD) | | |
| UTQFN-24L | 2 | W |
| TQFN-16 | 2 | W |
| Package thermal resistance, (θJA) (Note 2) | | |
| UTQFN-24L | 50 | °C/W |
| TQFN-16 | 51 | °C/W |
| Package thermal resistance, (θJC) | | |
| UTQFN-24L | 19 | °C/W |
| TQFN-16 | 25 | °C/W |
| | | |

Note 1: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 2: θJA is measured at 25°C ambient with the component mounted on a high effective thermal conductivity test board of JEDEC -51-7.

## 4.2 Recommended Operating Conditions

| Parameter | Rating | Unit |
|---|---|---|
| Input supply voltage (VDD) | +2.7 ~ +5.5 | V |
| VCONN voltage range | +2.7 ~ +5.5 | V |
| VBUS voltage | 0 ~ +20 | V |
| System I2C voltage range that SDA and SCL are pulled up to | +1.65 ~ +5.5 | V |
| Operating temperature range (TA) | 40 ~ +85 | °C |
| Junction temperature (TJ) | 40 ~ +125 | °C |
| | | |

## 4.3 Electrical Characteristics

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **General-Electrical Characteristics** | | | | | | |
| **Input Power** | | | | | | |
| VDD input voltage range | VVDD | | 2.7 | | 5.5 | V |
| VDD voltage rising release voltage | VBAT_UVLOR_LK(VTH) | DEAD_BAT_SEL, Reg.0xAC = 0x00 | | 2.8 | | V |
| VDD voltage falling lockout voltage | VBAT_UVLOF_LK(VTH) | DEAD_BAT_SEL, Reg.0xAC = 0x00 | | 2.6 | | V |
| VDD voltage lockout hysteresis voltage | VBAT_UVLOF_LK(HYS) | | | 200 | | mV |
| In dead battery mode, VBUS turn on voltage | VBUS_NMOS_ON | | 4 | | 6.5 | V |
| **N Channel MOSFET Gate Driver** | | | | | | |
| Sourcing current of SNKG (Note 3) | | VDD = 3.3V, VBUS = 5V | | 5.6 | | μA |
| Sourcing voltage (ON) between SNKG and SNKS (Note 3) | | | 5 | | 15 | V |
| Sourcing current of SRCG (Note 3) | | VDD = 3.3V, VBUS = 5V | | 5.6 | | μA |
| Sourcing voltage (ON) between SRCG and SRCS (Note 3) | | | 5 | | 15 | V |
| **Current Sense (IS+ and IS-)** | | | | | | |
| Current sense range | | R = 10mΩ | 0 | | 6.4 | A |
| Resolution | | R = 10mΩ | | 0.5 | | mV |
| Accuracy | | R = 10mΩ, I = 3A | 29.8 | 30 | 30.2 | mV |
| **GPIO0~GPIO2** | | | | | | |
| Logic-low threshold voltage for inputs | VIL_GPIO | | | | 1.97 | V |
| Logic-high threshold voltage for inputs | VIH_GPIO | | 2.6 | | | V |
| Logic-low threshold voltage for outputs | VOL_GPIO | IOL = -4mA | | | 0.4 | V |
| Logic-high threshold voltage for outputs | VOH_GPIO | IOH = 4mA | VDD - 0.4V | | | V |
| **Power Consumption** | | | | | | |
| UFP current consumption in unattached.SNK | I(UNATTACHED_UFP) | VDD = 3.3V | | 19 | | μA |
| DRP current consumption while toggling between unattached.SNK and unattached | I(UNATTACHED_DRP) | VDD = 3.3V | | 26 | | μA |
| DFP current consumption in unattached | I(UNATTACHED_DFP) | VDD = 3.3V | | 29 | | μA |
| UFP current consumption in attached.SNK active mode. PD disabled | I(ACTIVE_UFP) | VDD = 3.3V | | 1 | | mA |
| UFP current consumption in attached.SNK with PD enabled and transmitting continuous BIST carrier mode 2 | I(ACTIVE_UFP_PD) | VDD = 3.3V; TX_CARRIER_MODE2_SEL = 1 | | 5.2 | | mA |
| **Control Pins: INT_N** | | | | | | |
| INT_N leakage | I(INTN_LEAK) | VDD = 0V; 0 < INT_N < 3.3V | -1 | | 1 | μA |
| Low-level signal output voltage | VOL | IOL = -2mA | | | 0.4 | V |
| **I2C (SDA and SCL). VDD must be above 3V to operate at 3.3V I2C levels** | | | | | | |
| High-level input signal voltage | VIH(I2C) | | 1.2 | | | V |
| Low-level input signal voltage | VIL(I2C) | | | | 0.4 | V |
| Low-level signal output voltage (open-drain) | VOL(I2C) | | | | 0.4 | V |
| Low level output current | IOL(I2C) | | 6 | | | mA |
| Leakage through SDA and SCL pins | I(I2C_LKG) | VDD = 0V; pin pulled up to 3.6V | -1 | | 1 | μA |
| Capacitance for SDA and SCL pins | C(I2C) | | | | 10 | pF |

| | | | | | | |
|---|---|---|---|---|---|---|
| I2C bus capacitance for FM+ (1MHz) | C(I2C_FM+_BUS) | | | | 150 | pF |
| I2C bus capacitance for FM (400KHz) | C(I2C_FM_BUS) | | | | 150 | pF |
| External resistors on both SDA and SCL when operating at FM+ (1MHz) | R(EXT_I2C_FM+) | C(I2C_FM+_BUS) = 150pF | 620 | 820 | 910 | Ω |
| External resistors on both SDA and SCL when operating at FM (400KHz) | R(EXT_I2C_FM) | C(I2C_FM_BUS) = 150pF | 620 | 1500 | 2200 | Ω |
| **VBUS** | | | | | | |
| Bleed discharge is a low current discharge to provide a minimum load current if needed | R(Bleed) | | 8 | 10 | 12.5 | kΩ |
| Force discharge resistance | R (FA_Discharge) | | | 400 | | Ω |
| VBUS_voltage register measurement accuracy | V (VBUS_MEASURE_ACC) | | -2 | | 2 | % |
| **OTSD** | | | | | | |
| TJ over temperature trip threshold resulting in VCONN turn off and flag set | T(OTSD1) | | | 150 | | °C |
| **FBO Pin-QC mode** | | | | | | |
| Up/down current step (QC 2.0/3.0) | IUP, IDOWN | IUP = 40μA (9V), 70μA (12V), IDOWN = 14μA (3.6V). | | 2 | | μA |
| **USB Power Delivery- Electrical Characteristics** | | | | | | |
| **CC Pins (CC1 and CC2)** | | | | | | |
| Voltage on both CC pins when in dead battery and the attached DFP is presenting default current advertisement | VCC(USB_DB) | VDD = 0V | 0.25 | | 1.5 | V |
| Voltage on both CC pins when in dead battery and the attached DFP is presenting medium current (1.5A) advertisement | VCC(MED_DB) | VDD = 0V | 0.45 | | 1.5 | V |
| Voltage on both CC pins when in dead battery and the attached DFP is presenting high current (3.0A) advertisement | VCC(HIGH_DB) | VDD = 0V | 0.85 | | 2.45 | V |
| Pull-down resistor when in UFP or DRP mode | R(CC_RD) | VDD = 2.7V to 5.5V | 4.59 | 5.1 | 5.61 | kΩ |
| Pull-down resistor for active cable | R(CC_RA) | VDD = 2.7V to 5.5V | 0.8 | 1 | 1.2 | kΩ |
| Leakage current through CC pins | ICC(LKG) | VDD = 0V; VCONN = 0V; CC pin = 5.5V | | | 1.36 | mA |
| Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising default current source capability | V(UFP_CC_USB) | | 0.25 | | 0.61 | V |
| Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising medium (1.5A) current source capability | V(UFP_CC_MED) | | 0.7 | | 1.16 | V |
| Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising high (3.0A) current source capability | V(UFP_CC_HIGH) | | 1.31 | | 2.04 | V |
| Voltage threshold for detecting a UFP attach when the device is advertising default current source capability | VTH(DFP_CC_USB) | | 1.51 | 1.6 | 1.64 | V |
| Voltage threshold for detecting a UFP attach when the device is advertising medium current (1.5A) source capability | VTH(DFP_CC_MED) | | 1.51 | 1.6 | 1.64 | V |
| Voltage threshold for detecting a UFP attach when the device is advertising high current (3.0A) source capability | VTH(DFP_CC_HIGH) | | 2.46 | 2.6 | 2.74 | V |
| Voltage threshold for detecting a active cable attach when advertising default current | VTH(AC_CC_USB) | | 0.15 | 0.2 | 0.25 | V |
| Voltage threshold for detecting a active cable attach when advertising medium current | VTH(AC_CC_MED) | | 0.35 | 0.4 | 0.45 | V |
| Voltage threshold for detecting a active cable attach when advertising high current | VTH(AC_CC_HIGH) | | 0.76 | 0.8 | 0.84 | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| Default mode pull-up current source when advertising default current | ICC(DEFAULT_P) | | 64 | 80 | 96 | μA |
| Medium (1.5A) mode pull-up current source when advertising medium current | ICC(MED_P) | | 165.6 | 180 | 194.4 | μA |
| High (3.0A) mode pull-up current source when advertising high current | ICC(HIGH_P) | VDD > 3.0V | 303.6 | 330 | 356.4 | μA |
| Output impedance of CC1/CC2 during TX when operating in PD mode and driving the CC line (Note 3) | RTX(PD) | At 750KHz | 33 | 48 | 75 | Ω |
| Fast role swap request transmit driver resistance (excluding cable resistance) | RTX(FRS_PD) | | | | 5 | Ω |
| Transmit high voltage when operating in PD mode | VOH(PD) | | 1.05 | 1.125 | 1.2 | V |
| Transmit low voltage when operating in PD mode | VOL(PD) | | | | 0.07 | V |
| Receiver input impedance. Does not include pull-up or pull-down resistance from cable detect | RRX(PD) | TX is Hi-Z | 1 | | | MΩ |
| Fast role swap request voltage detection threshold | VRX(FRS_PD) | | 0.49 | 0.52 | 0.55 | V |
| Input high voltage when sourcing power. Selected when POWER_ROLE = 1 | VIH(PD_SRC) | | 0.8925 | | 1.5325 | V |
| Input high voltage when sinking power. Selected when POWER_ROLE = 0 | VIH(PD_SNK) | | 0.6425 | | 1.5325 | V |
| Input low voltage when sourcing power. Selected when POWER_ROLE = 1 | VIL(PD_SRC) | | -0.3325 | | 0.4825 | V |
| Input low voltage when sinking power. Selected when POWER_ROLE = 0 | VIL(PD_SNK) | | -0.3325 | | 0.2325 | V |
| External shunt capacitance on both CC1 and CC2 | CRX(SHUNT) | | 200 | | 450 | pF |
| **VCONN** | | | | | | |
| RON for VCONN power FET | RDS(ON) | | | 6 | 15 | Ω |
| Voltage to pass through VCONN power FET | V(PASS) | | | 5 | | V |
| VCONN current limit; VCONN is connected above this voltage | I(VCONN) | | 30 | 40 | 50 | mA |
| Threshold for detecting VCONN present | V(VCONN_PRES) | | | | 2.4 | V |
| Resistance to GND when VCONN discharge is enabled | R(VCONN_DIS) | | 4.59 | 5.1 | 5.61 | kΩ |
| **QC mode** | | | | | | |
| **High Voltage Dedicated Charging Port (HVDCP)** | | | | | | |
| Data detect voltage | VDAT(REF) | | 0.25 | 0.325 | 0.4 | V |
| Output voltage selection reference | VSEL_REF | | 1.8 | 2.0 | 2.2 | V |
| DM pull-down resistance | RD-(DWN) | | | 20 | | kΩ |
| DP leakage resistance | RDAT-LKG | VDD=3.2-6.4V, VD+=0.6-3.6V Switch SW1 = Off | 300 | 500 | 800 | kΩ |
| Switch SW1 on-resistance | RDS_ON_N1 | VDD = 5V, SW1 = 200μA | | | 40 | Ω |
| Data detect voltage | VDAT(REF) | | 0.25 | 0.325 | 0.4 | V |
| **Apple 2.4A mode** | | | | | | |
| DP_2.7V/DM_2.7V line output voltage | | VDD > 3V | 2.57 | 2.7 | 2.84 | V |
| DP_2.7V/DM_2.7V line output impedance | | VDD > 3V | | 33.6 | | kΩ |

Note 3: Not production tested.

# 5 Timing Requirements

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **General Timing Requirements** | | | | | | |
| **I2C (SDA and SCL)** | | | | | | |
| SCL clock frequency | FSCL | | 0.001 | | 1 | MHz |
| Hold time (repeated) start condition | tHD;STA | | 0.26 | | | µs |
| Low period of SCL | tLOW | | 0.5 | | | µs |
| High period of SCL | tHIGH | | 0.26 | | | µs |
| Setup time for a repeated start condition | tSU;STA | | 0.26 | | | µs |
| Data hold time | tHD;DAT | | 0 | | | µs |
| Data setup time | tSU;DAT | | 50 | | | µs |
| Setup time for STOP condition | tSU;STOP | | 0.26 | | | µs |
| Bus free time between STOP and START condition | tBUF | | 0.5 | | | µs |
| Data valid time | tVD;DAT | | | | 0.45 | µs |
| Data valid acknowledge time | tVD;ACK | | | | 0.45 | µs |
| Rise time of both SDA and SCL | tR_I2C | 30% to 70% | | | 120 | ns |
| Fall time of both SDA and SCL | tF_I2C | 70% to 30% | 14 | | 120 | ns |
| **Power-Up Requirements** | | | | | | |
| Time from VDD (min) to the device asserts INT_N low | tINT_N_LOW | Measured from VDD (min) to INT_N pin at VOL (min). | | | 4 | ms |
| VDD rise time | tVDD_RISE | Measured from 0V to VDD (min) | | | 40 | ms |
| **USB PD Timing** | | | | | | |
| **CC Pins (CC1 and CC2)** | | | | | | |
| Bit rate | Fbr_PD | | 270 | 300 | 330 | Kbps |
| Unit interval | tUI_PD | | 3.03 | 3.3 | 3.7 | µs |
| Rise time | tRISE_PD | 10% to 90%; CRX(SHUNT) = 200pF | 300 | | | ns |
| Fall time | tFALL_PD | 90% to 10%; CRX(SHUNT) = 200pF | 300 | | | ns |
| Rx Bandwidth limiting filter | tRxFilter | | 100 | | | ns |
| Time from the end of last bit of a frame until the state of the first bit of the next pre-amble | tInterFrameCap | | 25 | | 50 | ms |
| Time before the start of the first bit of the preamble when the transmitter shall start driving the line | tStartDrive | | -1 | | 1 | ms |
| Time to cease driving the line after the end of the last bit of a frame | tEndDriveBMC | | | | 23 | ms |
| Time to cease driving the line after the final high-to-low transition | tHoldLowBMC | | 1 | | 23 | µs |
| Transitions for signal detect | nTransitionCount | Number of transitions to be detected to declare bus non-idle | 3 | | | |
| Fast role swap request transmit duration | tFRSWAPTX | | 60 | | 120 | µs |
| Fast role swap detection time | tFRSWAPRX | | 30 | | 50 | µs |
| **VCONN Fault** | | | | | | |
| Delay from VCONN fault detected to VCONN fault status flag set | tVCONN_FAULT_DLY | | | | 20 | µs |
| Delay from VCONN fault detected to VCONN switch opened | tVCONN_OPEN | | | | 50 | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| **Sampling Timings** | | | | | | |
| Delay from VCONN fault detected to VCONN fault status flag set | tCC_SAMPLE_RATE | CC_SAMPLE_RATE = 2'b01 | | 2 | | ms |
| The sampling interval of VBUS voltage | tVBUSINRATE | CC_SAMPLE_RATE = 2'b01 | | 2 | | ms |
| **TCPC Timing Constraints** | | | | | | |
| Time between I2C STOP and first bit SOP | tBuffer2Cc | | | | 195 | µs |
| Time between last bit of EOP and Rx buffer ready | tCc2Buffer | | | | 50 | µs |
| Time between status change occurs and status register(s) updated | tSetReg | | | | 50 | µs |
| Time between status change occurs and status register(s) updated | tCcStatusDelay | | | | 200 | µs |
| Time from last I2C transaction or ALERT# pin assertion to entering Error Recovery (Watchdog function) | tHVWatchdog | | 650 | | 5000 | ms |
| | | | | | | |
| **QC Timing Requirements** | | | | | | |
| **High Voltage Dedicated Charging Port (HVDCP)** | | | | | | |
| DP high glitch filter time | TGLITCH(BC)-D+_H | | 1000 | 1250 | 1500 | ms |
| DM low glitch filter time | TGLITCH(BC)-D-_L | | | 1 | | ms |
| Output voltage glitch filter time | TGLITCH(V) CHANGE | | 20 | 40 | 60 | ms |
| Continuous mode glitch filter time | TGLITCH-CONT-CHANGE | | 100 | | 200 | µs |

# 6 Register

### Control and Status Register Field Definitions

| Access Type | Name | Description |
|---|---|---|
| R | Read | This field may be read by software. |
| W | Write | This field may be written by software. |
| C | Clear | This field may be cleared by a write '1'. Write '0' have no effect. |
| U | Update | This field may autonomously update by hardware. |

## 6.1 Vendor ID Low Byte Register (Address = 0x00)

Table 6-1 Vendor ID Low Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | VENDOR_ID_L | R | 0x5B | Low byte of a 16-bit USB-IF defined vendor ID of **0x00**. |

## 6.2 Vendor ID High Byte Register (Address = 0x01)

Table 6-2 Vendor ID High Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | VENDOR_ID_H | R | 0x2E | High byte of a 16-bit USB-IF defined vendor ID of **0x00**. |

## 6.3 Product ID Low Byte Register (Address = 0x02)

Table 6-3 Product ID Low Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | PRODUCT_ID_L | R | 0x06 | Low byte of a device 16-bit Product ID of **0x00**. |

## 6.4 Product ID High Byte Register (Address = 0x03)

Table 6-4 Product ID High Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | PRODUCT_ID_H | R | 0x66 | High byte of a device 16-bit Product ID of **0x00**. |

## 6.5 Device ID Low Byte Register (Address = 0x04)

Table 6-5 Device ID Low Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | DEVICE_ID_L | R | 0x00 | Low byte of a 16-bit Device ID. |

## 6.6 Device ID High Byte Register (Address = 0x05)

Table 6-6 Device ID High Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | DEVICE_ID_H | R | 0x00 | High byte of a 16-bit Device ID. |

## 6.7 USB Type-C Revision Low Byte Register (Address = 0x06)

Table 6-7 USB Type-C Revision Low Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | USBTYPEC_REV_L | R | 0x00 | Low byte of a 16-bit USB Type-C Revision. Revision 1.1. The device also supports USB Type-C Revision 1.2. |

## 6.8 USB Type-C Revision High Byte Register (Address = 0x07)

Table 6-8 USB Type-C Revision High Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 7:0 | USBTYPEC_REV_H | R | 0x00 | High byte of a 16-bit USB Type-C Revision. |

## 6.9 USB PD Revision Version Low Byte Register (Address = 0x08)

Table 6-9 USB PD Revision Version Low Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | USBPD_REV_VER_L | R | 0x11 | Low byte of a 16-bit USB PD version. Version 1.1. |

## 6.10 USB PD Revision Version High Byte Register (Address = 0x09)

Table 6-10 USB PD Revision Version High Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | USBPD_REV_VER_H | R | 0x30 | High byte of a 16-bit USB PD Revision. Revision 3.0. |

## 6.11 PD Interface Revision Low Byte Register (Address = 0x0A)

Table 6-11 PD Interface Revision Low Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | PD_INTERFACE_REV_L | R | 0x12 | Low byte of a 16-bit PD Interface (TCPC) Version. Version 1.2 |

## 6.12 PD Interface Revision High Byte Register (Address = 0x0B)

Table 6-12 PD Interface Revision High Byte Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | PD_INTERFACE_REV_H | R | 0x10 | High byte of a 16-bit PD Interface (TCPC) Revision. Revision 1.0 |

## 6.13 Alert High Byte Register (Address = 0x10)

If the UM3500F finishes the initiation, the PWR_STATUS bit will be set to high for informing the TCPM. When the UM3500F is powered on or reset, the default value of this register will be set to 0x02 caused by the PWR_STATUS bit.

This register is used to indicate a status change event. When a status change event occurs and its corresponding Alert mask is unmasked, the UM3500F will assert the INT_N low. The INT_N remains asserted until all events are cleared by write of 1'b1. Once all events are cleared or corresponding Alert mask is masked, the INT_N will be de-asserted high.

Table 6-13 Alert High Byte Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | VBUS_ALARM_HI | RCU | 0 | VBUS Voltage Alarm High<br>0b: Cleared<br>1b: A high-voltage alarm has occurred. Please refer to Reg.0x78 and Reg. 0x79 for setting high-voltage alarm level. |
| 6 | TX_SOP_SUCCESS | RCU | 0 | Transmit SOP* Message Successful<br>0b: Cleared<br>1b: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty. |
| 5 | TX_SOP_DISCARD | RCU | 0 | Transmit SOP* Message Discarded<br>0b: Cleared<br>1b: Reset or SOP* message transmission not sent due to incoming receive message. Transmit SOP* message buffer registers are empty. |
| 4 | TX_SOP_FAIL | RCU | 0 | Transmit SOP* Message Failed<br>0b: Cleared<br>1b: SOP* message transmission not successful, no ***GoodCRC*** response received on SOP* message transmission. Transmit SOP* message buffer registers are empty. |
| 3 | RX_HARD_RESET | RCU | 0 | Received Hard Reset<br>0b: Cleared.<br>1b: Received Hard Reset message |

| | | | | |
|---|---|---|---|---|
| 2 | RX_SOP_STATUS | RCU | 0 | Receive SOP* Message Status<br>0b: Cleared.<br>1b: Receive buffer register changed. RECEIVE_BYTE_COUNT (Reg.0x30) being set to 0 does not set this bit. |
| 1 | PWR_STATUS | RCU | 1 | Power Status<br>0b: Cleared.<br>1b: Power Status Changed |
| 0 | CC_STATUS | RCU | 0 | CC Status<br>0b: Cleared<br>1b: CC status changed |

## 6.14 Alert High Byte Register (Address = 0x11)

If the UM3500F is powered on or reset, the Reg.0x1F [7] will be set to high and all registers set to default. The Reg.0x11 [1] FAULT bit is therefore set high for informing TCPM. Consequently, the default value of this register is 0x02.

This register is used to indicate a status change event. When a status change event occurs and its corresponding Alert mask is unmasked, the UM3500F will assert the INT_N low. The INT_N remains asserted until all events are cleared by write of 1'b1. Once all events are cleared or corresponding Alert mask is masked, the INT_N will be de-asserted high.

Table 6-14 Alert Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | VENDOR_DEFINED_ALERT | RCU | 0 | Vendor Defined Alert: This bit can be cleared, regardless of the current status of the alert source.<br>0b: Cleared<br>1b: A vendor defined alert has been detected. Refer to the vendor interrupt register (Reg.0x90&91). |
| 6:4 | Reserved | R | 000 | Reserved |
| 3 | VBUS_SINK_DIS | RCU | 0 | VBUS Sink Disconnect Detected: This bit only be asserted when POWER_CONTROL.AUTO_DISCHARGE_DISCONNECT (Reg.0x1C[4]) is set<br>0b: Cleared<br>1b: A VBUS Sink Disconnect Threshold crossing has been detected |
| 2 | RX_BUF_OVR | RCU | 0 | Rx Buffer Overflow: Writing 1 to this register acknowledges the overflow. The overflow is cleared by writing to ALERT.ReceiveSOP*MessageStatus.<br>0b: Rx buffer is functioning properly.<br>1b: Rx buffer has overflowed. Future ***GoodCRC*** will not be sent. |
| 1 | FAULT | RCU | 1 | Fault<br>0b: No Fault<br>1b: A Fault has occurred. Read the FAULT_STATUS register (Reg.0x1F). |
| 0 | VBUS_ALARM_LO | RCU | 0 | VBUS Voltage Alarm Low<br>0b: Cleared<br>1b: A low-voltage alarm has occurred. Please refer to Reg.0x76 and Reg. 0x77 for setting low-voltage alarm level. |

## 6.15 Alert Mask Byte 0 Register (Address = 0x12)

This register controls whether a status change event in Alert register will cause the INT_N to be asserted low. When a specific event is masked, its corresponding status change event will not cause INT_N to be asserted low.

Table 6-15 Alert Mask Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | VBUS_ALARM_HI_MASK | RW | 1 | VBUS Voltage Alarm High Mask 0b: Interrupt masked<br>1b: Interrupt unmasked |
| 6 | TX_SOP_SUCCESS_MASK | RW | 1 | Transmit SOP* Message successful Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 5 | TX_SOP_DISCARD_MASK | RW | 1 | Transmit SOP* Message discarded Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |

| | | | | |
|---|---|---|---|---|
| 4 | TX_SOP_FAIL_MASK | RW | 1 | Transmit SOP* Message failed Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 3 | RX_HARD_RESET_MASK | RW | 1 | Received Hard Reset Message Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 2 | RX_SOP_STATUS_MASK | RW | 1 | Receive SOP* Message Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 1 | PWR_STATUS_MASK | RW | 1 | Power Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 0 | CC_STATUS_MASK | RW | 1 | CC Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |

## 6.16 Alert Mask Byte 1 Register (Address = 0x13)

This register controls if a status change event in Alert register will cause the INT_N to be asserted low. When a specific event is masked, its corresponding status change event will not cause INT_N to be asserted low.

Table 6-16 Alert Mask Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | VENDOR_DEFINED_ALERT_MASK | RW | 0 | Vendor Defined Alert Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 6:4 | Reserved | RW | 000 | Reserved |
| 3 | VBUS_SINK_DIS_MASK | RW | 1 | VBUS Sink Disconnect Detected Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 2 | RX_BUF_OVR_MASK | RW | 1 | Rx Buffer Overflow Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 1 | FAULT_MASK | RW | 1 | Fault Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 0 | VBUS_ALARM_LO_MASK | RW | 1 | VBUS Voltage Alarm Low Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |

## 6.17 Power Status Mask Register (Address = 0x14)

This register controls if a status change event in Alert register will cause the INT_N to be asserted low. When a specific event is masked, its corresponding status change event will not cause INT_N to be asserted low.

Table 6-17 Power Status Mask Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | DEBUG_ACCESSORY_MASK | RW | 1 | Debug Accessory Connected Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 6 | TCPC_INIT_STATUS_MASK | RW | 1 | TCPC Initialization Status Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 5 | SRC_HIGH_VBUS_STATUS_MASK | RW | 1 | Sourcing High Voltage Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 4 | SRC_VBUS_STATUS_MASK | RW | 1 | Sourcing VBUS Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 3 | VBUS_PRES_DET_STATUS_MASK | RW | 1 | VBUS Present Detection Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 2 | VBUS_PRES_INT_MASK | RW | 1 | VBUS Present Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |

| | | | | |
|---|---|---|---|---|
| 1 | VCONN_PRES_INT_MASK | RW | 1 | VCONN Present Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 0 | SINK_VBUS_STATUS_INT_MASK | RW | 1 | Sinking VBUS Status Interrupt Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |

## 6.18 Fault Status Mask Register (Address = 0x15)

This register controls if a status change event in Alert register will cause the INT_N to be asserted low. When a specific event is masked, its corresponding status change event will not cause INT_N to be asserted low.

Table 6-18 Fault Status Mask Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | ALLREG_RESET_TO_DEFAULT_MASK | RW | 1 | All Registers Reset to Default Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 6 | FORCE_VBUS_MASK | RW | 1 | Force Off VBUS Interrupt Status Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 5 | AUTO_DISC_FAIL_MASK | RW | 1 | Auto Discharge Failed Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 4 | FORCE_DISC_FAIL_MASK | RW | 1 | Force Discharge Failed Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 3 | VBUS_OCP_FAIL_STATUS_MASK | RW | 1 | Internal or External OCP VBUS Over Current Protection Fault Interrupt Status Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 2 | VBUS_OVP_FAIL_STATUS_MASK | RW | 1 | Internal or External OVP VBUS Over Voltage Protection Fault Interrupt Status Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 1 | VCONN_OCP_FAULT_STATUS_MASK | RW | 1 | VCONN Over Current Fault Interrupt Status Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |
| 0 | I2C_INT_ERR_STATUS_I_MASK | RW | 1 | I2C Interface Error Interrupt Status Mask<br>0b: Interrupt masked<br>1b: Interrupt unmasked |

## 6.19 TCPC Control Register (Address = 0x19)

The TCPM writes to the TCPC_ CONTROL register to set the Plug Orientation and enable/disable clock stretching.

Table 6-19 TCPC Control Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | Reserved | RW | 00 | Reserved |
| 5 | EN_WATCHDOG_TIMER | RW | 0 | Enable Watchdog Timer<br>Required if DEVICE_CAPABILITIES_2 WatchDog Timer (Reg.0x27 [0]) = 1b<br>0b: Watchdog Monitoring is disabled (default)<br>1b: Watchdog Monitoring is enabled |
| 4 | DEBUG_ACC_CTL | RW | 0 | Debug Accessory Control<br>0b: Controlled by the device (power on default)<br>1b: Controlled by TCPM. The TCPM writes 1b to this register to take over control of asserting the DebugAccessoryConnected#. |
| 3:2 | I2C_CLOCK_STRETCHING_CTL | RW | 00 | The device does not support clock stretching. |

| | | | | |
|---|---|---|---|---|
| 1 | BIST_TEST_MODE | RW | 0 | Built in Self-Test Mode:<br>Setting this bit to 1 is intended to be used only when a USB compliance tester is using USB BIST Test Data to test the PHY layer of the device. The TCPM should clear this bit when a detach is detected.<br>0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert.<br>1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but will not be passed to the TCPM via Alert. |
| 0 | PLUG_ORIENTATION | RW | 0 | Plug Orientation<br>0b: When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled.<br>1b: When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. |

## 6.20 Role Control Register (Address = 0x1A)

The TCPM writes to this register to configure the CC pull up (Rp) or pull down (Rd) resistors.

Table 6-20 Role Control Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | RW | 0 | Reserved |
| 6 | DRP | RW | 0 | Dual-Role Power:<br>The TCPC toggles CC1 & CC2 after receiving COMMAND.Look4Connection and until a connection is detected. Upon connection, the TCPC shall resolve to either an Rp or Rd and report the CC1/CC2 State in the CC_STATUS register.<br>0b: No DRP. Bits [3:0] determine Rp/Rd/Ra or open settings<br>1b: DRP |
| 5:4 | RP_VALUE | RW | 00 | Pull up resistor<br>00b: Rp default current<br>01b: Rp 1.5 A<br>10b: Rp 3 A<br>11b: Reserved |
| 3:2 | CC2 | RW | 10 | Configuration Channel 1<br>00b: Ra<br>01b: Rp<br>10b: Rd<br>11b: Open (Disconnect or don't care) |
| 1:0 | CC1 | RW | 10 | Configuration Channel 2<br>00b: Ra<br>01b: Rp<br>10b: Rd<br>11b: Open (Disconnect or don't care) |

## 6.21 Fault Control Register (Address = 0x1B)

The TCPM writes to FAULT_CONTROL to enable/disable FAULT circuitry.

Table 6-21 Fault Control Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:5 | Reserved | RW | 000 | Reserved |
| 4 | FORCE_OFF_VBUS | RW | 0 | The device does not support the function. |
| 3 | VBUS_DIS_FAULT_DETECT_TIMER | RW | 0 | VBUS Discharge Fault Detection Timer: This enables or disables the timers for both FAULT_STATUTS.AutoDischargeFailed (Reg.0x1F [5]) and FAULT_STATUS.ForceDischargeFailed (Reg.0x1F [4]).<br>0b: VBUS Discharge Fault Detection Timer enabled<br>1b: VBUS Discharge Fault Detection Timer disabled |
| 2 | VBUS_OCP_FAULT | RW | 0 | The device does not support the function. |
| 1 | VBUS_OVP_FAULT | RW | 0 | The device does not support the function in this field. Please refer to the Reg. 0xCC. When the VBUS is higher than the specified voltage, the Reg. 0xCD [1] will be written with a 1b and the GPIO 2 (fault pin) will be pulled high. |
| 0 | VCONN_OC_FAULT | RW | 0 | VCONN Over Current Fault:<br>Required if DEVICE_CAPABILITIES_2. VCONNOvercurrentFaultCapable (Reg.0x26 [0]) = 1b.<br>0b: Fault detection circuit enabled<br>1b: Fault detection circuit disabled |

## 6.22 Power Control Register (Address = 0x1C)

Table 6-22 Power Control Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | RW | 0 | Reserved |
| 6 | VBUS_VOLTAGE_MONITOR | RW | 1 | VBUS Voltage Monitor: Controls only VBUS VOLTAGE Monitoring. VBUS_VOLTAGE will report all zeroes if disabled. Required if DEVICE_CAPABILITIES_1. VBUS Measurement and Alarm Capable (Reg.0x25 [2]) = 1b.<br>0b: VBUS_VOLTAGE Monitoring is enabled.<br>1b: VBUS_VOLTAGE Monitoring is disabled (default). |
| 5 | DISABLE_VOTAGE_ALARMS | RW | 1 | Disable Voltage Alarms: Controls VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. Required if DEVICE_CAPABILITIES_1. VBUS Measurement and Alarm Capable (Reg.0x25 [2]) = 1b.<br>0b: Voltage Alarms Power status reporting is enabled.<br>1b: Voltage Alarms Power status reporting is disabled (default). |
| 4 | AUTO_DISCHARGE_DISCONNECT | RW | 0 | Auto Discharge Disconnect<br>Setting this bit in a Source TCPC triggers the following actions upon disconnection detection:<br>1.Disable sourcing power over VBUS<br>2.VBUS discharge<br>Sourcing power over VBUS shall be disabled before or at same time as starting VBUS discharge.<br><br>Setting this bit in a Sink TCPC triggers the following action upon disconnection detection:<br>1. VBUS discharge<br>The device will automatically disable discharge once the voltage on VBUS is below vSafe0V (max) or VBUS_STOP_DISCHARGE_THRESHOLD (Reg.0x74 & 0x75).<br>0b: The device shall not automatically discharge VBUS based on VBUS voltage. (Default)<br>1b: The device will automatically discharge |
| 3 | EN_BLEED_DISCHARGE | RW | 0 | Enable Bleed Discharge:<br>Bleed Discharge is a low current discharge to provide a minimum load current. The device will apply 10 Ohms on VBUS for bleed discharge. Required if DEVICE_CAPABILITIES_1. BleedDischarge (Reg.0x25 [4]) = 1b<br>0b: Disable bleed discharge (default)<br>1b: Enable bleed discharge of VBUS |
| 2 | FORCE_DISCHARGE | RW | 0 | Force Discharge:<br>When this field is set, the device will discharge VBUS to Vsafe0V or threshold programmed in the VBUS_STOP_DISCHARGE_THRESHOLD register (Reg.0x74 & 0x75). Once VBUS is discharged to desired level, the device will disable the Force Discharge. Required if DEVICE_CAPABILITIES_1.ForceDischarge (Reg.0x25 [3])= 1b<br>0b: Disable forced discharge (default).<br>1b: Enable forced discharge of VBUS. |
| 1 | Reserved | RW | 0 | Reserved |
| 0 | ENABLE_VCONN | RW | 0 | Enable VCONN<br>0b: Disable VCONN Source (default)<br>1b: Enable VCONN Source to CC indicated by PLUG_ORIENTATION in TCPC Control register (Reg0x19 [0]). |

## 6.23 CC Status Register (Address = 0x1D)

The CC status register indicate the state of the UM3500F. It is set by the UM3500F and read by the TCPM. The CC status register is not latched and is continually updated unless powered off.

Table 6-23 CC Status Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | Reserved | R | 00 | Reserved |

| | | | | |
|---|---|---|---|---|
| 5 | LOOKING4CONNECTION | RU | 0 | Looking for Connection<br>0b: The device is not actively looking for a connection. A transition from '1' to '0' indicates a potential connection has been found.<br>1b: The device is looking for a connection (toggling as a DRP or looking for a connection as Sink/Source only condition) |
| 4 | CONNECT_RESULT | RU | 1 | Connect Result<br>0b: the device is presenting Rp<br>1b: the device is presenting Rd |
| 3:2 | CC2_STATE | RU | 00 | If (ROLE_CONTROL.CC2=Rp) or (CONNECT_RESULT=0)<br>00b: SRC.Open (Open, Rp)<br>01b: SRC.Ra (below maximum vRa)<br>10b: SRC.Rd (within the vRd range)<br>11b: reserved<br><br>If (ROLE_CONTROL.CC2=Rd) or (CONNECT_RESULT=1)<br>00b: SNK.Open (Below maximum vRa)<br>01b: SNK.Default (Above minimum vRd-Connect)<br>10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A<br>11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A<br><br>If ROLE_CONTROL.CC2=Ra, this field is set to 00b<br>If ROLE_CONTROL.CC2=Open, this field is set to 00b<br><br>This field always returns 00b if (Looking4Connection=1) or (POWER_CONTROL.ENABLE_VCONN=1 and TCPC_CONTROL.PLUG_ORIENTATION =0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2. |
| 1:0 | CC1_STATE | RU | 00 | If (ROLE_CONTROL.CC1 = Rp) or (CONNECT_RESULT=0)<br>00b: SRC.Open (Open, Rp)<br>01b: SRC.Ra (below maximum vRa)<br>10b: SRC.Rd (within the vRd range)<br>11b: reserved<br><br>If (ROLE_CONTROL.CC1 = Rd) or (CONNECT_RESULT=1)<br>00b: SNK.Open (Below maximum vRa)<br>01b: SNK.Default (Above minimum vRd-Connect)<br>10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp- 1.5A<br>11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp- 3.0A<br><br>If ROLE_CONTROL.CC1=Ra, this field is set to 00b<br>If ROLE_CONTROL.CC1=Open, this field is set to 00b<br><br>This field always returns 00b if (Looking4Connection=1) or (POWER_CONTROL.ENABLE_VCONN=1 and TCPC_CONTROL.PLUG_ORIENTATION =1). Otherwise, the returned value depends upon ROLE_CONTROL.CC1. |

## 6.24 Power Status Register (Address = 0x1E)

The power status register indicates the state of the UM3500F. It is set by the UM3500F and read by the TCPM. The power status register is not latched and is continually updated unless powered off.

Table 6-24 Power Status Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | DEBUG_ACC_CONNECTED | RU | 0 | Debug Accessory Connected: Reflects the state of the DebugAccessoryConnected# output if supported.<br>0b: No Debug Accessory connected (default)<br>1b: Debug Accessory connected |
| 6 | TCPC_INIT_STATUS | RU | 0 | TCPC Initialization Status<br>0b: The device has completed initialization and all registers are valid.<br>1b: The device is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh. |
| 5 | SOURCING_HIGH_VOLTAGE | RU | 0 | The Device does not support the function in this field. Please refer to vendor defined register. The VBUS control function is assigned to the Reg.0xD0~0xD2. |
| 4 | SOURCING_VBUS | RU | 0 | The Device does not support the function in this field. Please refer to vendor defined register. The VBUS control function is assigned to the Reg.0xD0~0xD2. |

| | | | | |
|---|---|---|---|---|
| 3 | VBUS_PRES_DETECT_ENABLED | RU | 0 | VBUS Present Detection Enabled:<br>Indicates if the device is monitoring for VBUS Present or if the circuit has been powered off.<br>0b: VBUS Present Detection Disabled (Default)<br>1b: VBUS Present Detection Enabled |
| 2 | VBUS_PRESENT | RU | 0 | VBUS present:<br>The device shall report VBUS present when it detects VBUS rises above 4 V.<br>The device shall report VBUS is not present when it detects VBUS falls below 3.5 V.<br>The device may report VBUS is not present if VBUS is between 3.5 V and 4 V.<br>0b: VBUS Disconnected<br>1b: VBUS Connected |
| 1 | VCONN_PRESENT | RU | 0 | VCONN present:<br>If POWER_CONTROL.EnableVCONN (Reg.0x1C [0]) is disabled VCONN Present should be set to 0b.<br>0b: VCONN is not present<br>1b: This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4 V |
| 0 | SINKING_VBUS | RU | 0 | The device does not support the function in this field. Please refer to the Reg.0x85 [1] NMOS_SNK_ON. It is used to control sinking power path. |

## 6.25 Fault Status Register (Address = 0x1F)

The fault status register indicates the state of the UM3500F. It is set by the UM3500F and read by the TCPM. The fault status register is latched unless powered off.

The UM3500F indicates a fault status change has occurred by presenting a logical 1 in the corresponding bit position in this register, presenting a logical 1 to the ALERT.Fault bit (Reg.0x11 [1]), and asserting the INT_N pin if the corresponding fault bit in FAULT_STATUS_MASK (Reg.0x15) is 1 and ALERT_MASK.Fault (Reg.0x13 [1]) is 1. The TCPM clears the FAULT bit by writing a logical 1 to the respective FAULT bit position and then writing a logical 1 to the ALERT.Fault bit (Reg.0x11 [1]) after all bits in FAULT_STATUS (Reg.0x1F) has been cleared. The TCPM writing a logical 0 to any FAULT bit has no effect and therefore does not cause those FAULT bits to be set or cleared.

Table 6-25 Fault Status Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | ALLREG_RESET_TO_DEFAUL T | RCU | 1 | All Registers Reset to Default:<br>This bit is asserted when the device resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs.<br>0b: Cleared<br>1b: All registers had been reset to default value |
| 6 | FORCE_OFF_VBUS_STATUS | RCU | 0 | The device does not support this function. |
| 5 | AUTO_DIS_FAIL_STATUS | RCU | 0 | Auto Discharge Failed:<br>If POWER_CONTROL.AutoDischargeDisconnect (Reg.0x1C [4]) is set, the device will report discharge fails if VBUS is not below vSafe0V within tSafe0V.<br>0b: No discharge failure<br>1b: Discharge commanded by the TCPM failed |
| 4 | FORCE_DIS_FAIL_STATUS | RCU | 0 | Force Discharge Failed:<br>If POWER_CONTROL.ForceDischarge (Reg.0x1C [2]) is set, the device will report a discharge fails if VBUS is not below vSafe0V within tSafe0V.<br>0b: No discharge failure<br>1b: Discharge commanded by the TCPM failed |
| 3 | VBUS_OCP_FAULT_STATUS | RCU | 0 | The device does not support this function. |
| 2 | VBUS_OVP_FAULT_STATUS | RCU | 0 | The device does not support this function. |
| 1 | VCONN_OCP_FAULT_STATUS | RCU | 0 | VCONN Over Current Fault:<br>Required if DEVICE_CAPABILITIES_2.VCONNOvercurrentFaultCapable (Reg.0x26 [0]) = 1b<br>0b: No Fault detected<br>1b: Over current VCONN fault latched |

| | | | | |
|---|---|---|---|---|
| 0 | I2C_INT_ERROR_STATUS | RCU | 0 | I2C Interface Error:<br>A TRANSMIT has been sent with an empty TRANSMIT_BUFFER. May be asserted if a non-zero value has been written to a reserved bit in a register.<br>0b: No Error<br>1b: I2C error has occurred |

## 6.26 Command Register (Address = 0x23)

The Command is issued by the TCPM. The Command is cleared by the UM3500F after being acted upon.

Table 6-26 Command Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | COMMAND | RWU | 0x00 | 1001 1001b: Look4Connection<br>Start DRP Toggling if ROLE_CONTROL.DRP (Reg.0x1A [6]) =1b. If ROLE_CONTROL.CC1/CC2 (Reg.0x1A [1:0]/[3:2]) = 01b start with Rp, if ROLE_CONTROL.CC1/CC2 (Reg.0x1A [1:0]/[3:2]) =10b start with Rd.<br>If ROLE_CONTROL.CC1/CC2 (Reg.0x1A [1:0]/[3:2]) are not both 01b or 10b, then do not start toggling.<br>The TCPM shall issue COMMAND.Look4Connection to enable the device to restart Connection Detection in cases where the ROLE_CONTROL contents will not change. An example of this is when a potential connection as a Source occurred but was further debounced by the TCPM to find the Sink disconnected. In this case a Source Only or DRP should go back to its Unattached.Src state. This would result in ROLE_CONTROL staying the same.<br><br>Besides command 0x99, the device will accept others command but will do nothing with it. |

## 6.27 Device Capabilities 1 Byte 0 Register (Address = 0x24)

This register is in the nonvolatile memory of the UM3500F. This register describes features supported by the UM3500F.

Table 6-27 Device Capabilities 1 Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:5 | ROLES_SUPPORTED | R | 110 | Roles Supported.<br>000b: USB Type-C Port Manager can configure the Port as Source only or sink only (not DRP)<br>001b: Source only 010b: Sink only<br>011b: Sink with accessory support<br>100b: DRP only<br>101b: Source, Sink, DRP, Adapter/Cable all supported<br>110b: Source, Sink, DRP<br>111b: Not valid |
| 4 | SOP_DBG_SUPPORT | R | 1 | SOP'_DBG/SOP"_DBG Support<br>Configured in RECEIVE_DETECT (Reg.0x2F) and TRANSMIT (Reg.0x50)<br>0b: All SOP* except SOP'_DBG/SOP"_DBG<br>1b: All SOP* messages are supported |
| 3 | SRC_VCONN | R | 1 | Source VCONN<br>Support for POWER_CONTROL.EnableVCONN (Reg.0x1C [0]) and POWER_STATUS.VCONNPresent (Reg.0x1E [1]) implemented.<br>0b: The device is not capable of switching VCONN<br>1b: The device is capable of switching VCONN |
| 2 | SNK_VBUS | R | 0 | This field does not affect the device. Please refer to the Reg.0x85 [1] NMOS_SNK_ON. It is used to control sinking power path. |
| 1 | SRC_ HIGH_VBUS | R | 0 | This field does not affect the device. Please refer to vendor defined register. The VBUS control function is assigned to the Reg.0xD0~0xD2. |
| 0 | SRC_VBUS | R | 0 | This field does not affect the device. Please refer to vendor defined register. The VBUS control function is assigned to the Reg.0xD0~0xD2. |

## 6.28 Device Capabilities 1 Byte 1 Register (Address = 0x25)

This register is in the nonvolatile memory of the UM3500F. This register describes features supported by the UM3500F.

Table 6-28 Device Capabilities 1 Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | R | 0 | Reserved |
| 6 | VBUS_OCP_REPORT | R | 0 | VBUS OCP Reporting<br>Support for both FAULT_STATUS.InternalorExternalOCP (Reg.0x1F [3]) and FAULT_CONTROL. InternalorExternalOCP (Reg.0x1B [2]) implemented.<br>0b: VBUS OCP is not reported by the device<br>1b: VBUS OCP is reported by the device |
| 5 | VBUS_OVP_REPORT | R | 0 | This field does not affect the device. Please refer to the Reg. 0xCC. When the VBUS is higher than the specified voltage, the Reg. 0xCD [1] will be written with a 1b and the GPIO 2 (fault pin) will be pull high. |
| 4 | BLEED_DISCHARGE | R | 1 | Bleed Discharge<br>Support for POWER_CONTROL.EnableBleedDischarge (Reg.0x1C [3]) implemented.<br>0b: No Bleed Discharge implemented in the device<br>1b: Bleed Discharge is implemented in the device |
| 3 | FORCE_DISCHARGE | R | 1 | Force Discharge<br>Support for POWER_CONTROL.ForceDischarge (Reg.0x1C [2]), FAULT_STATUS.ForceDischargeFailed (Reg.0x1F [4]), and VBUS_STOP_DISCHARGE_THRESHOLD (Reg.0x74&0x75) implemented.<br>Support for VBUS_STOP_DISCHARGE_THRESHOLD (Reg.0x74&0x75) register implemented when act as Source.<br>0b: No Force Discharge implemented in the device<br>1b: Force Discharge is implemented in the device |
| 2 | VBUS_MEASURE_ALARM_CAPABLE | R | 1 | VBUS Measurement and Alarm Capable<br>Support for VBUS_VOLTAGE, VBUS_VOLTAGE_ALARM_HI_CFG (Reg.0x76&0x77), VBUS_VOLTAGE_ALARM_LO_CFG (Reg.0x78&0x79) implemented.<br>0b: No VBUS voltage measurement or VBUS Alarms<br>1b: VBUS voltage measurement and VBUS Alarms |
| 1:0 | SRC_RESISTOR_SUPPORT | R | 10 | Source Resistor Supported<br>Rp values which may be configured by the TCPM via the ROLE_CONTROL register (Reg.0x1A).<br>00b: Rp default only<br>01b: Rp 1.5 A and default<br>10b: Rp 3 A, 1.5 A, and default<br>11b: Reserved |

## 6.29 Device Capabilities 2 Byte 0 Register (Address = 0x26)

This register is in the nonvolatile memory of the UM3500F. This register describes features supported by the UM3500F.

Table 6-29 Device Capabilities 2 Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SINK_DISCON NECT_DETECT | R | 1 | Sink Disconnect Detection<br>0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented (Use POWER_STATUS.VbusPresent (Reg.0x1E [2]) = 0b to indicate a Sink disconnect)<br>1b: VBUS_SINK_DISCONNECT_THRESHOLD implemented |
| 6 | STOP_DISCHARGE_THRESHOLD | R | 1 | Stop Discharge Threshold<br>0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented 1b: VBUS_STOP_DISCHARGE_THRESHOLD implemented |

| | | | | |
|---|---|---|---|---|
| 5:4 | VBUS_VOLTAGE_ALARM_LSB | R | 00 | VBUS Voltage Alarm LSB<br>00b: The device has 25mV LSB for its voltage alarm and uses all10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG<br>01b: The device has 50mV LSB for its voltage alarm and uses only 9 bits VBUS_VOLTAGE_ALARM_HI_CFG [0] and VBUS_VOLTAGE_ALARM_LO_CFG [0] are ignored by the device<br>10b: The device has 100mV LSB for its voltage alarm and uses only 8 bits VBUS_VOLTAGE_ALARM_HI_CFG [1:0] and VBUS_VOLTAGE_ALARM_LO_CFG [1:0] are ignored by the device<br>11b: Reserved<br>Support for VBUS_VOLTAGE_ALARM_LO_CFG and VBUS_VOLTAGE_ALARM_HI implemented |
| 3:1 | VCONN_PWR_SUPPORT | R | 000 | VCONN Power Supported<br>000b: 100m W |
| 0 | VCONN_OC_FAULT_SUPPOR T | R | 1 | VCONN Overcurrent Fault Capable<br>Support for FAULT_STATUS.VCONNOverCurrentFault (Reg.0x1F [1]) and FAULT_CONTROL.VCONNOverCurrentFault (Reg.0x1B [0]) implemented<br>0b: The device is not capable of detecting a VCONN fault<br>1b: The device is capable of detect a VCONN fault |

## 6.30 Device Capabilities 2 Byte 1 Register (Address = 0x27)

This register is in the nonvolatile memory of the UM3500F. This register describes features supported by the UM3500F.

Table 6-30 Device Capabilities 2 Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | Reserved | R | 0x00 | Reserved |
| 0 | WATCHDOG_TIMER | R | 1 | Watchdog Timer<br>0b: TCPC_CONTROL.Enable Watchdog Timer (Reg.0x19 [5]) not implemented<br>1b: TCPC_CONTROL.Enable Watchdog Timer (Reg.0x19 [5]) implemented |

## 6.31 Standard Input Capabilities Register (Address = 0x28)

This register is in the nonvolatile memory of the UM3500F. This register describes the optional normative Standard Inputs and their capability.

Table 6-31 Standard Input Capabilities Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:3 | Reserved | R | 0x00 | Reserved |
| 2 | EXT_VBUS_OVF_SUPPORT | R | 0 | VBUS External Over Voltage Fault<br>0b: Not present in the device<br>1b: Present in the device |
| 1 | EXT_VBUS_OCF_SUPPORT | R | 0 | VBUS External Over Current Fault<br>0b: Not present in the device<br>1b: Present in the device |
| 0 | EXT_FORCE_OFF_VBUS_SUP PORT | R | 0 | Force Off VBUS (Source or Sink)<br>0b: Not present in the device<br>1b: Present in the device |

## 6.32 Standard Output Capabilities Register (Address = 0x29)

This register is in the nonvolatile memory of the UM3500F. This register describes the optional normative Standard Inputs and their capability.

Table 6-32 Standard Output Capabilities Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | R | 0 | Reserved |

| | | | | |
|---|---|---|---|---|
| 6 | DEBUG_ACC_INDICATOR | R | 0 | Debug Accessory Indicator<br>0b: Not present in the device<br>1b: Present in the device |
| 5 | VBUS_PRESENT_MONITOR | R | 0 | VBUS Present Monitor<br>0b: Not present in the device<br>1b: Present in the device |
| 4 | AUDIO_ADAP_ACC_INDICATOR | R | 0 | Audio Adapter Accessory Indicator<br>0b: Not present in the device<br>1b: Present in the device |
| 3 | ACTIVE_CABLE_ INDICATOR | R | 0 | Active Cable Indicator<br>0b: Not present in the device<br>1b: Present in the device |
| 2 | MUX_CONFIG_CONTROL | R | 0 | MUX Configuration Control<br>0b: Not present in the device<br>1b: Present in the device |
| 1 | CONNECT_PRESENT | R | 0 | Connection Present<br>0b: Not present in the device<br>1b: Present in the device |
| 0 | CONNECTOR_ORIENT | R | 0 | Connector Orientation<br>0b: Not present in the device<br>1b: Present in the device |

## 6.33 Message Header Info Register (Address = 0x2E)

The UM3500F shall set this register at power on. The TCPM may overwrite this register after UM3500F initialization is complete.
On attach and after implementing the tCCDebounce, the TCPM shall update the MESSAGE_HEADER_INFO Register first before writing to the RECEIVE_DETECT (Reg.0x2F) register.
The UM3500F reads from this register to generate the Message header for the GoodCRC.

Table 6-33 Message Header Info Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:5 | Reserved | R | 000 | Shall be set to zero by sender and ignored by receiver |
| 4 | CABLE_PLUG | RW | 0 | Cable Plug<br>0b: Message originated from Source, Sink, or DRP<br>1b: Message originated from a Cable Plug |
| 3 | DATA_ROLE | RW | 0 | Data Role<br>0b: UFP<br>1b: DFP |
| 2:1 | USBPD_SPECREV | RW | 01 | USB PD Specification Revision<br>00b: Revision 1.0<br>01b: Revision 2.0<br>10b: Revision 3.0<br>11b: Reserved |
| 0 | POWER_ROLE | RW | 0 | Power Role<br>0b: Sink<br>1b: Source |

## 6.34 Receiver Detect Register (Address = 0x2F)

The TCPM notifies the UM3500F of the message type and/or signaling types to be detected. The TCPM should not set any bits in this register until it is able to respond. The UM3500F responds to the enabled message type with a GoodCRC if it is a SOP* message, except in the case of a GoodCRC message.
On Hard Reset reception, the UM3500F shall set the RECEIVE_DETECT bits to zero to disable automatic transmission of GoodCRC . On detection of a Disconnect, the TCPC shall set the RECEIVE_DETECT bits all to zero to disable automatic transmission of GoodCRC. The UM3500F shall set the RECEIVE_DETECT bits to zero to disable automatic transmission of GoodCRC when RECEIVE_DETECT.CableReset is set and a Cable Reset is received.

Table 6-34 Receiver Detect Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | RW | 0 | Shall be set to zero by sender and ignored by receiver |
| 6 | EN_CABLE_RESET | RW | 0 | Enable Cable Reset<br>0b: The device does not detect Cable Reset signaling (default)<br>1b: The device detects Cable Reset signaling |

| | | | | |
|---|---|---|---|---|
| 5 | EN_HARD_RESET | RW | 0 | Enable Hard Reset<br>0b: The device does not detect Hard Reset signaling (default)<br>1b: The device detects Hard Reset signaling |
| 4 | EN_SOP_DBGPP | RW | 0 | Enable SOP_DBG'' Message<br>0b: The device does not detect SOP_DBG'' message (default)<br>1b: The device detects SOP_DBG'' message |
| 3 | EN_SOP_DBGP | RW | 0 | Enable SOP_DBG' Message<br>0b: The device does not detect SOP_DBG' message (default)<br>1b: The device detects SOP_DBG' message |
| 2 | EN_SOPPP_MESSAGE | RW | 0 | Enable SOP'' Message<br>0b: The device does not detect SOP'' message (default)<br>1b: The device detects SOP'' message |
| 1 | EN_SOPP_MESSAGE | RW | 0 | Enable SOP' Message<br>0b: The device does not detect SOP' message (default)<br>1b: The device detects SOP' message |
| 0 | EN_SOP_MESSAGE | RW | 0 | Enable SOP Message<br>0b: The device does not detect SOP message (default)<br>1b: The device detects SOP message |

## 6.35 Receive Byte Count Register (Address = 0x30)

The TCPM reads the RECEIVE_BYTE_COUNT to determine the number of bytes in the RX_BUFFER_DATA_OBJECT (Reg.0x34~0x4F) and the RX_BUF_FRAME_TYPE (Reg.0x31) to determine the type of message.
The TCPM then reads the information in the RX_BUF_HEADER (Reg.0x32~33) and the RX_BUFFER_DATA_OBJECT. The UM3500F shall set the RECEIVE_BYTE_COUNT to 0 after the interrupt has been cleared.
Upon detection of a Disconnect, the UM3500F shall set the RECEIVE_BYTE_COUNT to zero.

Table 6-35 Receive Byte Count Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | RECEIVE_BYTE_COUNT | RU | 0x00 | Receive Byte Count<br>Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register. This is the number of bytes in the RX_BUFFER_DATA_OBJECTS plus three (for the RX_BUF_FRAME_TYPE (Reg.0x31) and RX_BUF_HEADER (Reg.0x32~0x33)). |

## 6.36 Receive Buffer Frame Type Register (Address = 0x31)

Table 6-36 Receive Buffer Frame Type Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:3 | Reserved | R | 0x00 | Shall be set to zero by sender and ignored by receiver |
| 2:0 | RX_SOP_MESSAGE | RU | 000 | Received SOP* Message<br>000b: Received SOP<br>001b: Received SOP'<br>010b: Received SOP''<br>011b: Received SOP_DBG'<br>100b: Received SOP_DBG''<br>110b: Received Cable Reset<br>All others are reserved |

## 6.37 Receive Buffer Header Byte 0 Register (Address = 0x32)

Table 6-37 Receive Buffer Header Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | RX_BUF_HDR_BYTE_0 | RU | 0x00 | Receive Buffer Header Byte 0<br>Byte 0 (bits 7:0) of USB PD message header. |

## 6.38 Receive Buffer Header Byte 1 Register (Address = 0x33)

Table 6-38 Receive Buffer Header Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 7:0 | RX_BUF_HDR_BYTE_1 | RU | 0x00 | Receive Buffer Header Byte 1<br>Byte 1 (bits 15:8) of USB PD message header. |

## 6.39 Receive Buffer Data Object 1~7 Register (Address = 0x34 ~ 0x4F)

Table 6-39 Receive Buffer Data Object 1 Through 7 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | RX_BUFF_OBJn_BYTE_m | RU | 0x00 | Receive Buffer Data Object n Byte m (**n: 1~7; m: 0 ~3**)<br>Ex: RX_BUFF_OBJ1_BYTE_0 = Byte 0 (bits 7..0) of 1st data object. |

- Address 0x34: RX_BUFF_OBJ1_BYTE_0, Byte 0 (bits 7..0) of 1st data object.
- Address 0x35: RX_BUFF_OBJ1_BYTE_1, Byte 1 (bits 15..8) of 1st data object.
- Address 0x36: RX_BUFF_OBJ1_BYTE_2, Byte 2 (bits 23..16) of 1st data object.
- Address 0x37: RX_BUFF_OBJ1_BYTE_3, Byte 3 (bits 31..24) of 1st data object.
- …
- Address 0x4F: RX_BUFF_OBJ7_BYTE_3, Byte 3 (bits 31..24) of 7th data object.

## 6.40 Transmit Register (Address = 0x50)

The TCPM writes to this register to transmit a SOP* message where the SOP* message payload is in 51h..6Fh registers. The entire register shall be written at once and then sent. The TCPC shall clear the TRANSMIT register (Reg.0x50) and TRANSMIT_BYTE_COUNT (Reg.0x51) after executing the transmission regardless of success or failure.

Table 6-40 Transmit Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | Reserved | RW | 00 | Shall be set to zero by sender and ignored by receiver |
| 5:4 | RETRY_COUNTER | RW | 00 | Retry Counter<br>00b: No message retry is required<br>01b: Automatically retry message transmission once<br>10b: Automatically retry message transmission twice<br>11b: Automatically retry message transmission three times |
| 3 | Reserved | RW | 0 | Shall be set to zero by sender, shall be ignored by receiver |
| 2:0 | TX_SOP_MESSAGE | RW | 000 | Transmit SOP* Message<br>000b: Transmit SOP<br>001b: Transmit SOP' 010b: Transmit SOP"<br>011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG''<br>101b: Transmit Hard Reset 110b: Transmit Cable Reset<br>111b: Transmit BIST Carrier Mode 2 |

## 6.41 Transmit Byte Count Register (Address = 0x51)

The TRANSMIT_BUFFER holds the TRANSMIT_BYTE_COUNT (Reg.0x51), the TX_BUF_HEADER (Reg.0x52~53), and the TX_BUFFER_DATA_OBJECTS (Reg.0x54~0x6F) (SOP* payload).

Table 6-41 Transmit Byte Count Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | TX_BYTE_COUNT | RWU | 0x00 | Transmit Byte Count<br>The number of bytes the TCPM will write. This is the number of bytes in the TX_BUFFER_DATA_OBJECTS (Reg.0x54~6F) plus two (for the TX_BUF_HEADER (Reg.0x52~53)). |

## 6.42 Transmit Buffer Header Byte 0 Register (Address = 0x52)

Table 6-42 Transmit Buffer Header Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | TX_BUF_HDR_BYTE_0 | RW | 0x00 | Transmit Buffer Header Byte 0<br>Byte 0 (bits 7:0) of USB PD message header. |

## 6.43 Transmit Buffer Header Byte 1 Register (Address = 0x53)

Table 6-43 Transmit Buffer Header Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | TX_BUF_HDR_BYTE_1 | RW | 0x00 | Transmit Buffer Header Byte 1<br>Byte 1 (bits 15:8) of USB PD message header. |

## 6.44 Transmit Buffer Data Object 1~7 Register (Address = 0x54 ~ 0x6F)

Table 6-44 Transmit Buffer Data Object 1 Through 7 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | TX_BUFF_OBJn_BYTE_m | R | 0 | Transmit Buffer Data Object n Byte m (**n: 1~7; m: 0 ~3**)<br>Ex: TX_BUFF_OBJ1_BYTE_0 = Byte 0 (bits 7...0) of 1st data object. |

- Address 0x54: TX_BUFF_OBJ1_BYTE_0 / (Extend header Byte 0), Byte 0 (bits 7..0) of 1st data object.
- Address 0x55: TX_BUFF_OBJ1_BYTE_1 / (Extend header Byte 1), Byte 1 (bits 15..8) of 1st data object.
- Address 0x56: TX_BUFF_OBJ1_BYTE_2, Byte 2 (bits 23..16) of 1st data object.
- Address 0x57: TX_BUFF_OBJ1_BYTE_3, Byte 3 (bits 31..24) of 1st data object.
- …
- Address 0x6F: TX_BUFF_OBJ7_BYTE_3, Byte 1 (bits 31..24) of 7th data object.

## 6.45 VBUS Voltage Byte 0 Register (Address = 0x70)

The TCPM may read this register to determine the VBUS voltage measured on the Source or Sink at the Type-C Connector. The UM3500F shall maintain synchronization between the upper and lower 8 bits of the register.

Table 6-45 VBUS Voltage Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | VBUS_MEASUREMENT[7:0] | RU | 0x00 | VBUS Voltage Measurement [7:0]<br>VBUS_MEASUREMENT[9:0] = VBUS_MEASUREMENT[9:8] + VBUS_MEASUREMENT[7:0]. The LSB is 25mV. |

## 6.46 VBUS Voltage Byte 1 Register (Address = 0x71)

Table 6-46 VBUS Voltage Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:2 | Reserved | R | 0x00 | Reserved |
| 1:0 | VBUS_MEASUREMENT[9:8] | RU | 0 | VBUS Voltage Measurement[9:8]<br>VBUS_MEASUREMENT[9:0] = VBUS_MEASUREMENT[9:8] + VBUS_MEASUREMENT[7:0]. The LSB is 25mV. |

## 6.47 VBUS Sink Disconnect Threshold Byte 0 Register (Address = 0x72)

This register is required by UM3500F which act as a Sink and are capable of receiving voltages greater than vSafe5V. Implementation of this register shall be defined in DEVICE_CAPABILITIES_2.SinkDisconnectDetection (Reg.0x26 [7]). This register has no action for a Source. The TCPM writes to this register to set the threshold at which a Sink will start the Auto Discharge if it is in the Attached.SNK state.

Table 6-47 VBUS Sink Disconnect Threshold Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | VBUS_SNK_DISC_THRESHOLD[7:0] | RW | 0x00 | VBUS Sink Disconnect Threshold[7:0]<br>10-bit for voltage threshold with 25 mV LSB. (Default vSafe5V) ±5% accuracy. A value of bit 9..0 = 0x00 disables this threshold. |

## 6.48 VBUS Sink Disconnect Threshold Byte 1 Register (Address = 0x73)

Table 6-48 VBUS Sink Disconnect Threshold Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:2 | Reserved | R | 0x00 | Reserved |

| | | | | |
|---|---|---|---|---|
| 1:0 | VBUS_SNK_DISC_THRESHOLD[9:8] | RW | 00 | VBUS Sink Disconnect Threshold[9:8]<br>10-bit for voltage threshold with 25 mV LSB. (Default vSafe5V) ±5% accuracy. A value of bit 9..0 = 0x00 disables this threshold. |

## 6.49 VBUS Stop Discharge Threshold Byte 0 Register (Address = 0x74)

This register is required by UM3500F which act as a Source and support POWER_CONTROL.ForceDischarge (Reg.0x1C [2]). The TCPM writes to this register to set the threshold at which a Source shall stop the forced discharge when POWER_CONTROL.ForceDischa rge (Reg.0x1C [2]) = 1b. TCPC acting as a Source shall always discharge to vSafe0V upon disconnect, Hard Reset, or Power Role Swap.

Table 6-49 VBUS Stop Discharge Threshold Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | VBUS_STOP_DISCHARGE_THRESHOLD[7:0] | RW | 0x00 | VBUS Stop Discharge Threshold[7:0]<br>10-bit for voltage threshold with 25 mV LSB. (Default vSafe5V) ±5% accuracy. |

## 6.50 VBUS Stop Discharge Threshold Byte 1 Register (Address = 0x75)

Table 6-50 VBUS Stop Discharge Threshold Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:2 | Reserved | R | 0x00 | Reserved |
| 1:0 | VBUS_STOP_DISCHARGE_THRESHOLD[9:8] | RW | 00 | VBUS Stop Discharge Threshold[9:8]<br>10-bit for voltage threshold with 25 mV LSB. (Default vSafe5V) ±5% accuracy. |

## 6.51 VBUS Voltage Alarm High Configure Byte 0 Register (Address = 0x76)

The TCPM writes to this register to set the high voltage alarm level. The UM3500F sets ALERT. VBUS Voltage Alarm High (Reg.0x10 [7]) to 1 when VBUS exceeds the over voltage level. These registers are required if it is reported as supported in the one of the DEVICE_CAPABILITES registers (Reg.0x25 [2]).

Table 6-51 VBUS Voltage Alarm High Configure Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | VBUS_ALARM_HIGH_THRESHOLD[7:0] | RW | 0x00 | VBUS Alarm High Threshold[7:0]<br>10-bit for voltage threshold with 25 mV LSB. ±5% accuracy. |

## 6.52 VBUS Voltage Alarm High Configure Byte 1 Register (Address = 0x77)

Table 6-52 VBUS Voltage Alarm High Configure Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:2 | Reserved | R | 0x00 | Reserved |
| 1:0 | VBUS_ALARM_HIGH_THRESHOLD[9:8] | RW | 0x00 | VBUS Alarm High Threshold [9:8]<br>10-bit for voltage threshold with 25 mV LSB. ±5% accuracy. |

## 6.53 VBUS Voltage Alarm Low Configure Byte 0 Register (Address = 0x78)

The TCPM writes to this register to set the low voltage alarm level. The UM3500F sets ALERT. VBUS Voltage Alarm Low (Reg.0x11 [0]) to 1 when VBUS drops below the undervoltage level. These registers are required if it is reported as supported in the one of the DEVICE_CAPABILITES registers (Reg.0x25 [2]).

Table 6-53 VBUS Voltage Alarm Low Configure Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | VBUS_ALARM_LOW_THRESHOLD[7:0] | RW | 0x00 | VBUS Alarm Low Threshold [7:0]<br>10-bit for voltage threshold with 25 mV LSB. ±5% accuracy. |

## 6.54 VBUS Voltage Alarm Low Configure Byte 1 Register (Address = 0x79)

Table 6-54 VBUS Voltage Alarm Low Configure Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:2 | Reserved | R | 0x00 | Reserved |

| | | | | |
|---|---|---|---|---|
| 1:0 | VBUS_ALARM_LOW_THRESHOLD[9:8] | RW | 0x00 | VBUS Alarm Low Threshold [9:8]<br>10-bit for voltage threshold with 25 mV LSB. ±5% accuracy. |

## 6.55 System Control Byte 0 (Address = 0x80)

Table 6-55 System Control Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:3 | Reserved | RW | 00010 | Reserved |
| 2 | OTSD_EN | RW | 0 | Enable Over Temperature Shutdown<br>1b: Enable on die thermal diode function<br>0b: Disable on die thermal diode function |
| 1 | INT_VCONNDIS_DIS | RW | 0 | Disable Internal VCONN Discharge<br>1b: Disable VCONN discharge function<br>0b: Set auto turn on VCONN discharge function |
| 0 | INT_VBUSDIS_DIS | RW | 0 | Disable Internal VBUS Discharge<br>1b: Disable VBUS discharge function<br>0b: Set auto turn on VBUS discharge function |

## 6.56 System Control Byte 1 Register (Address = 0x81)

Table 6-56 System Control Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | Reserved | RW | 00 | Reserved |
| 5 | VBUS_DET_EN | RW | 0 | Enable VBUS Detection<br>1b: Enable VBUS detect (to AIP)<br>0b: Disable VBUS detect (to AIP) |
| 4 | VCONN_DET_EN | RW | 0 | Enable VCONN Detection<br>1b: Enable VCONN detect (to AIP)<br>0b: Disable VCONN detect (to AIP) |
| 3 | Reserved | RW | 0 | Reserved |
| 2 | TX_CARRIER_MODE2_SEL | RW | 0 | Transmit Carrier Mode 2 Selection<br>1b: The device shall continuously send BIST carrier mode 2 data when the BIST carrier mode 2 is issued.<br>0b: The device will stop to send BIST carrier mode 2 data at 45ms when<br>BIST carrier mode 2 is issued. |
| 1 | QC_SRC_RST | W | 0 | Reset QC source and SCP Function<br>This bit is written by TCPM and automatically cleared by the device.<br>0b: Maintain the original QC source status.<br>1b: Reset QC source & SCP |
| 0 | TX_FAST_ROLE_SWAP_ST | RW | 0 | Transmit Fast Role Swap Start<br>This field is used to execute the fast role swap when the role of the device is transmitter.<br>0b: Stop fast role swap<br>1b: Start fast role swap |

## 6.57 Debug Function Byte 1 Register (Address = 0x82)

Table 6-57 System Control Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CC2_DIS | RW | 1 | Disable Configuration Channel 2<br>0b: Enable CC2 detection.<br>1b: Disable CC2 detection. |
| 6 | CC1_DIS | RW | 1 | Disable Configuration Channel 1<br>0b: Enable CC1 detection.<br>1b: Disable CC1 detection. |
| 5:0 | Reserved | RW | 0x00 | Reserved |

## 6.58 Mode Status Byte 0 Register (Address = 0x83)

Table 6-58 Mode Status Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 7:4 | QC_MODE_STATUS | R | 0x0 | QC Mode Status<br>It is used to monitor the situation of QC source.<br>0000b: IDLE<br>0001b: Reserved<br>0010b: Reserved<br>0011b: DIV_MODE (Apple 2.4A Mode)<br>0100b: Reserved<br>0101b: DCP<br>0110b: Reserved<br>0111b: TRY_QC<br>1000b: DLY_40ms<br>1001b: QC_MODE_5V<br>1010b: QC_MODE_CONT<br>1011b: QC_MODE_9V<br>1100b: QC_MODE_12V<br>1101b: QC_MODE_20V<br>1110b: QC_MODE_UNDEF<br>1111b: QC_FCP_MODE |
| 3:2 | Reserved | R | 00 | Reserved |

## 6.59 Mode Status Byte 1 Register (Address = 0x84)

Table 6-59 Mode Status Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | R | 0 | Reserved |
| 6 | VCONN_OTSD_FLAG | R | 0 | VCONN Over Temperature Shutdown Flag<br>This function is valid if VCONN is applied to CC pin. When the temperature of the VCONN switch is higher than the 160°C, the VCONN switch will be automatically turned off until the temperature decreases to 130°C.<br>0b: No VCONN over temperature.<br>1b: VCONN switch occurs over temperature. |
| 5:0 | Reserved | R | 0x00 | Reserved |

## 6.60 External NMOS Control Register (Address = 0x85)

Table 6-60 External NMOS Control Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | DEAD_BAT_OFF | RW | 0 | Disable Dead Battery<br>0b: Enable dead battery supported.<br>1b: Disable dead battery supported. |
| 6:2 | Reserved | R | 0x00 | Reserved |
| 1 | NMOS_SNK_ON | RW | 0 | Turn on Sink NMOS<br>TCPM writes this bit to control the sink NMOS driver for turning on or turning off.<br>0b: Disable VBUS power on sinking connector port.<br>1b: Enable VBUS power on sinking connector port. |
| 0 | NMOS_SRC_ON | RW | 0 | Turn on Source NMOS<br>TCPM writes this bit to control the source NMOS driver for turning on or turning off.<br>0b: Disable VBUS power on sourcing connector port.<br>1b: Enable VBUS power on sourcing connector port. |

## 6.61 System Control Byte 2 Register (Address = 0x86)

Table 6-61 System Control Byte 2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | Reserved | RW | 00 | Reserved |
| 5:4 | Reserved | RW | 00 | Reserved |
| 3 | FASTROLE_RX_EN | RW | 0 | Enable Receive Fast Role Swap<br>This field is used to enable receive fast role swap when the role of the device is receiver (only sink device).<br>0b: Fast role swap detect disable<br>1b: Fast role swap detect enable |
| 2 | Reserved | RW | 0 | Reserved |
| 1:0 | Reserved | RW | 00 | Reserved |

## 6.62 Vendor Interrupts Byte 0 Register (Address = 0x90)

This register is used to indicate a status change event. When a status change event occurs and its corresponding Alert mask is unmasked, the UM3500F will assert the INT_N low. The INT_N remains asserted until all events are cleared by write of 1'b1. Once all events are cleared or corresponding Alert mask is masked, the INT_N will be de-asserted high.

For example, if Reg.0x13 [7] VENDOR_DEFINED_ALERT_MASK and the corresponding vendor interrupts mask (Reg.0x92 & 0x93) are written 1b for unmasking, the INT_N will assert low when UM3500F occurs vendor interrupt event. The TCPM should examine what the vendor interrupt event (Reg.0x91 & 0x92) occurs and deal with it.

Table 6-62 Vendor Interrupts Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | RCU | 0 | Reserved |
| 6 | Reserved | RCU | 0 | Reserved |
| 5 | Reserved | RCU | 0 | Reserved |
| 4 | I_ADC_VOLT_UPDATE | RCU | 0 | ADC Voltage Update Interrupt<br>0b: Cleared.<br>1b: The device has finished the voltage ADC and the data of ADC has stored with corresponding register (Reg.0xC1~0xC2). If the data of ADC is different from previous one, this bit will be change to 1b. TCPM can access the data of ADC while this bit changes to 1b. |
| 3 | I_VCONN_OC | RCU | 0 | VCONN Over Current Interrupt<br>0b: No VCONN OC<br>1b: Over-current event occurs on VCONN |
| 2 | I_VCONN_OTSD_OCCUR | RCU | 0 | VCONN Over Temperature Shutdown Occur<br>0b: No OTSD<br>1b: Over temperature event occurs in VCONN switch |
| 1 | Reserved | RCU | 0 | Reserved |
| 0 | I_FAST_ROLE_SWAP_OCCUR | RCU | 0 | Fast Role Swap Occur Interrupt<br>0b: Cleared<br>1b: Fast role swap request received |

## 6.63 Vendor Interrupts Byte 1 Register (Address = 0x91)

This register is used to indicate a status change event. When a status change event occurs and its corresponding Alert mask is unmasked, the UM3500F will assert the INT_N low. The INT_N remains asserted until all events are cleared by write of 1'b1. Once all events are cleared or corresponding Alert mask is masked, the INT_N will be de-asserted high.

For example, if Reg.0x13 [7] VENDOR_DEFINED_ALERT_MASK and the corresponding vendor interrupts mask (Reg.0x92 & 0x93) are written 1b for unmasking, the INT_N will assert low when UM3500F occurs vendor interrupt event. The TCPM should examine what the vendor interrupt event (Reg.0x91 & 0x92) occurs and deal with it.

Table 6-63 Vendor Interrupts Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:5 | Reserved | RCU | 000 | Reserved |
| 4 | I_ OV_EVENT | RCU | 0 | Over Voltage Event Interrupt<br>0b: No over voltage on CC/DP/DM/VBUS pin.<br>1b: Over voltage event occur on CC/DP/DM/VBUS pin. |
| 3 | Reserved | RCU | 0 | Reserved |
| 2 | I_ADC_CUR_UPDATE | RCU | 0 | ADC Current Update Interrupt<br>0b: ADC is converting.<br>1b: The device has finished the current ADC and the data of ADC has stored with corresponding register (Reg.0xC3~0xC4). If the data of ADC is different from previous one, this bit will be change to 1b. TCPM can access the data of ADC while this bit changes to 1b. |
| 1 | Reserved | RCU | 0 | Reserved |
| 0 | I_QC_ST_CHG | RCU | 0 | QC Mode Status Change Interrupt<br>0b: Cleared<br>1b: The QC mode status has been changed by the device. TCPM could check the value of Reg.0x83 [7:4]. |

## 6.64 Vendor Interrupts Mask Byte 0 Register (Address = 0x92)

Table 6-64 Vendor Interrupts Mask Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | RW | 0 | Reserved |
| 6 | Reserved | RW | 0 | Reserved |
| 5 | Reserved | RW | 0 | Reserved |
| 4 | I_ADC_VOLT_UPDATE_MASK | RW | 0 | ADC Voltage Update Interrupt Mask<br>0b: Disable interrupt<br>1b: Enable interrupt |
| 3 | I_VCONN_OC_MASK | RW | 0 | VCONN Over Current Interrupt Mask<br>0b: Disable interrupt<br>1b: Enable interrupt |
| 2 | I_VCONN_OTSD_MASK | RW | 0 | Over Temperature Interrupt Mask<br>0b: Disable interrupt<br>1b: Enable interrupt |
| 1 | Reserved | RW | 0 | Reserved |
| 0 | I_FAST_ROLE_SWAP_MASK | RW | 0 | Fast Role Swap Interrupt Mask<br>0b: Disable interrupt<br>1b: Enable interrupt |

## 6.65 Vendor Interrupts Mask Byte 1 Register (Address = 0x93)

Table 6-65 Vendor Interrupts Mask Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:5 | Reserved | RW | 000 | Reserved |
| 4 | I_CC_OV _MASK | RW | 0 | CC Over Voltage Interrupt Mask<br>0b: Disable interrupt<br>1b: Enable interrupt |
| 3 | Reserved | RW | 0 | Reserved |
| 2 | I_ADC_CUR_UPDATE_MASK | RW | 0 | ADC Current Update Interrupt Mask<br>0b: Disable interrupt<br>1b: Enable interrupt |
| 1 | Reserved | RW | 0 | Reserved |
| 0 | I_QC_ST_CHG_MASK | RW | 0 | QC Mode Status Change Mask<br>0b: Disable interrupt<br>1b: Enable interrupt |

## 6.66 CC General Control Register (Address = 0x94)

Table 6-66 CC General Control Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | RW | 0 | Reserved |
| 6 | PD_TXRX_RESET | W | 0 | Reset PD Transmit and Receive:<br>Both PD TX and RX state machines are reset when TCPM writes this field with a 1b. This bit is written by TCPM and automatically cleared by the device.<br>0b: No operation<br>1b: Reset PD engine |
| 5 | GLOBAL_FW_RESET | W | 0 | Global Reset:<br>The device will be reset to power on default when TCPM writes this field with a 1b. This bit is written by TCPM and automatically cleared by the device.<br>0b: No operation<br>1b: Global reset |
| 4 | AUTO_DRP_SAMPLE_CTRL | RW | 0 | Auto DRP Sample Control:<br>When the device is enabled for autonomous DRP toggle, this field controls when CC pins are sampled while unattached.<br>0b: Continuously checks CC pins based on CC_SAMPLE_RATE field (Reg.0x97 [3:2]).<br>1b: Only checks CC pins just before Role toggle. |
| 3:2 | CC_SAMPLE_RATE | RW | 01 | CC Sample Rate:<br>This field controls the device CC pins sample rate.<br>00b: 1ms<br>01b: 2ms<br>10b: 8ms<br>11b: 16ms |

| | | | | |
|---|---|---|---|---|
| 1:0 | DRP_DUTY_CYCLE | RW | 00 | DRP Duty Cycle<br>00b: 30%, total scan time = 50 ms<br>01: 50%, total scan time = 70 ms<br>10: 56.25%, total scan time = 80 ms<br>11b: 65%, total scan time = 100 ms |

## 6.67 MTP Control Byte 0 Register (Address = 0x98)

Table 6-67 MTP Control Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | MTP_RELOAD_OFF | RW | 0 | MTP Reload Disable<br>When this field is set to 1b, the Dead Battery Function (Reg.0x85 [7]) and Dead Battery Voltage (Reg.0xAC) default setting could not be changed. Even with Global Reset (Reg.0x94 [5]) could not be changed.<br>0b: MTP Reload enable<br>1b: MTP Reload disable |
| 6:5 | Reserved | RW | 00 | Reserved |
| 4 | MTP_REG_WREN | RW | 0 | MTP Register Write Enable<br>The MTP registers are locked by this field. The MTP registers could be changed if TCPM writes this field with a 1b.<br>0b: Register write disable<br>1b: Register write enable |
| 3 | Reserved | R | 0 | Reserved |
| 2 | MTP_WRITE | RW | 0 | MTP Program Trigger<br>TCPM writes the data to MTP register firstly and TCPM writes this field with a 1b. The MTP register is therefore changed.<br>0b: No operation<br>1b: Program MTP |
| 1 | MTP_ERASE | RW | 0 | MTP Erase Trigger<br>TCPM selects MTP register that want to erase firstly and TCPM writes this field with a 1b. The MTP register is therefore erased.<br>0b: No operation<br>1b: Erase MTP |
| 0 | MTP_READ | RW | 0 | MTP Read Trigger<br>TCPM writes this field with a 1b, then, the MTP registers could be read.<br>0b: No operation<br>1b: Read MTP |

## 6.68 MTP Control Byte 1 Register (Address = 0x99)

Table 6-68 MTP Control Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | MTP_ERASE_TYPE | RW | 0 | MTP Erase Type:<br>MTP Chip / Page Erase<br>0b: Chip Erase<br>1b: Page Erase |
| 6:4 | MTP_ERASE_PAGE | RW | 000 | MTP Page Erase:<br>The MTP page erase function is locked by the password. The password must be filled in the MTP_PASSWORD [7:0] (Reg.0x9A). The page from 2 to 7 make public to the customers and the password is B7h. However, both page 0 and page 1 are reserved by vendor.<br>000b: Erase page 0<br>001b: Erase page 1<br>010b: Erase page 2<br>011b: Erase page 3<br>100b: Erase page 4<br>101b: Erase page 5<br>110b: Erase page 6<br>111b: Erase page 7 |
| 3 | MTP_WRITE_TYPE | RW | 0 | MTP Write Type:<br>MTP Chip / Page Program<br>0b: Chip Program<br>1b: Page Program |

| | | | | |
|---|---|---|---|---|
| 2:0 | MTP_WRITE_PAGE | RW | 000 | MTP Page Program:<br>The MTP page program function is locked by the password. The password must be filled in the MTP_PASSWORD [7:0] (Reg.0x9A). The page from 2 to 7 make public to the customers and the password is B7h. However, both page 0 and page 1 are reserved by vendor.<br>000b: Program page 0<br>001b: Program page 1<br>010b: Program page 2<br>011b: Program page 3<br>100b: Program page 4<br>101b: Program page 5<br>110b: Program page 6<br>111b: Program page 7 |

## 6.69 MTP Password Register (Address = 0x9A)

Table 6-69 MTP Password Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | MTP_PASSWORD | RW | 0x00 | MTP Password<br>The customer password is B7h for chip program / erase and page program / erase. |

## 6.70 QC Protocol Control Byte 0 Register (Address = 0x9C)

Table 6-70 QC Protocol Control Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | QC_SRC_DIS | RW | 1 | Qualcomm Quick Charge Disable<br>0b: QC source enable<br>1b: QC source disable |
| 6 | HVDCP_DIS | RW | 1 | Qualcomm Quick Charge Disable<br>0b: with HVDCP function<br>1b: No HVDCP function (default 5V) |
| 5 | QC3.0_DIS | RW | 0 | Qualcomm Quick Charge 3.0 Disable (SRC only)<br>0b: QC 3.0 continuous mode enable<br>1b: QC 3.0 continuous mode disable |
| 4 | QC2.0_DIS | RW | 0 | Qualcomm Quick Charge 2.0 Disable (SRC only)<br>0b: QC 2.0 mode enable<br>1b: QC 2.0 mode disable |
| 3 | Reserved | RW | 0 | Reserved |
| 2 | SCP_FCP_DIS | RW | 0 | Huawei Super Charge/Fast Charge Protocol Disable (SRC only)<br>0b: SCP/FCP mode enable<br>1b: SCP/FCP mode disable |
| 1 | Reserved | RW | 0 | Reserved |
| 0 | PD_DIS | RW | 0 | USB PD Disable (SRC/SNK)<br>0b: PD enable<br>1b: PD disable |

## 6.71 QC Protocol Control Byte 1 Register (Address = 0x9D)

Table 6-71 QC Protocol Control Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | FBO_SCC_SEL | RW | 0 | FBO pin Sink/Source Current Selection:<br>The VBUS control of the device is implemented by sourcing/sinking current from FBO pin. The scale of FBO pin sourcing/sinking current is determined by feedback resistance of power stage.<br>0b: The upper feedback resistance of power stage is 50k Ohm.<br>1b: The upper feedback resistance of power stage is 100k Ohm. |
| 6 | Reserved | RW | 0 | Reserved |
| 5 | Reserved | RW | 0 | Reserved |
| 4 | FBO_CTRL | RW | 0 | Feedback Output Node Control:<br>The device utilizes the feedback pin of the power stage to obtain the VBUS voltage control.<br>0b: Disable FBO pin to control the power stage<br>1b: Enable FBO pin to control the power stage |

| | | | | |
|---|---|---|---|---|
| 3 | QC_CLASS_CTRL | RW | 0 | Quick Charge (SRC only) QC source class A enable<br>0b: Class B enable (QC 2.0 5V, 9V, 12V, 20V)<br>1b: Class A enable (QC 2.0 5V, 9V, 12V) |
| 2 | Reserved | RW | 0 | Reserved |
| 1 | Reserved | RW | 0 | Reserved |
| 0 | QC_H_VOLT_CTRL | RW | 0 | Quick Charge (SRC only) QC source 12V disable<br>0b: 12V enable (QC 2.0 5V, 9V, 12V, 20V)<br>1b: 12V disable (QC 2.0 5V, 9V) |

## 6.72 Dead Battery Voltage Selection Register (Address = 0xAC)

Table 6-72 Dead Battery Voltage Selection Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:3 | Reserved | R | 0x00 | Reserved |
| 2:0 | DEAD_BATTERY_SEL | RW | 000 | Dead Battery Voltage Selection:<br>Suppose TCPM writes this field with a 000b. the device is supplied by VDD and NMOS_SNK_ON (Reg.0x85 [1]) is automatically disabled by the device when VDD is larger than 2.8V. However, the device is supplied by VBUS and NMOS_SNK_ON (Reg.0x85 [1]) is enabled automatically by the device when VDD is lower than 2.6V. In this manner, the dead battery function in the device is therefore implemented.<br>000b: Dead Battery Voltage 2.6V. Rising 2.8V<br>001b: Dead Battery Voltage 2.8V. Rising 3.0V<br>010b: Dead Battery Voltage 3.0V. Rising 3.2V<br>011b: Dead Battery Voltage 2.6V. Rising 3.0V<br>100b: Dead Battery Voltage 2.8V. Rising 3.2V |

## 6.73 ADC Control Register (Address = 0xC0)

Table 6-73 ADC Control Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Reserved | RW | 1 | Reserved |
| 6:5 | TM_DRIVE_SEL | RW | 00 | TM Pin Drive current:<br>The scale of current from TM pin could be selected by this field. The TM pin current is used to drive the connected thermal resistance. The voltage on the thermal resistance is therefore converted to temperature by ADC_TEMP_DATA (Reg.0xC4).<br>00b: 1.25uA<br>01b: 5uA<br>10b: 20uA<br>11b: 100uA |
| 4:3 | ADC_DEBOUNCE_TIME | RW | 00 | ADC Debounce Time:<br>00b: 0 time<br>01b: 1 time<br>10b: 2 times<br>11b: 3 times |
| 2:0 | ADC_SCAN_TIME | RW | 001 | ADC Scan Time:<br>This field is used to decide how often to do an ADC conversion.<br>000b: 4ms<br>001b: 8ms<br>010b: 16ms<br>011b: 32ms<br>100b: 64ms<br>101b: 128ms |

## 6.74 ADC IBUS Data Register (Address = 0xC3)

Table 6-74 ADC IBUS Data Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 7:0 | ADC_IBUS_DATA | R | 0x00 | ADC IBUS Data:<br>This field shows the current flowing from IS+ pin to IS− pin. The value of current measurement could be obtained by the following equation.<br><br>IBUS = ADC_IBUS_DATA / (1992.1875*Rs)<br><br>Where IBUS is the current flowing from IS+ pin to IS− pin. Rs is the resistance between IS+ pin and IS− pin.<br>If Rs is equation to 10m Ohm, the equation is therefore rearranged as follow:<br>IBUS = ADC_IBUS_DATA *50.19608mA |

## 6.75 ADC Temperature Data Register (Address = 0xC4)

Table 6-75 ADC Temperature Data Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | ADC_TEMP_DATA | R | 0x00 | ADC Temperature Data:<br>The value of voltage on TM pin measurement is presented in this field. The TM pin must be connected to the thermal resistor and the selected current of TM pin (Reg.0xC0 [6:5]) will flow to the thermal resistor. This field could represent analog voltage ranging from 0.4V to 2.4V. Each bit of this field can be calculated as 9.41176471mV. Additionally, the converted temperature is according to the different thermal resistor and TM_DRIVE_SEL (Reg.0xC0 [6:5]) selected by the customer. |

## 6.76 GPIO Direction Control Register (Address = 0xC8)

Table 6-76 GPIO Direction Control Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:3 | Reserved | R | 0x00 | Reserved |
| 2 | GPIO2_DIR_CTRL | RW | 0 | GPIO2 Direction Control<br>0b: Input<br>1b: Output |
| 1 | GPIO1_DIR_CTRL | RW | 0 | GPIO1 Direction Control<br>0b: Input<br>1b: Output |
| 0 | GPIO0_DIR_CTRL | RW | 0 | GPIO0 Direction Control<br>0b: Input<br>1b: Output |

## 6.77 GPIO Output Data Register (Address = 0xC9)

Table 6-77 GPIO Output Data Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:3 | Reserved | R | 0x00 | Reserved |
| 2 | GPIO2_OUTPUT_DATA | RW | 0 | GPIO2 Output Data<br>The direction of GPIO2 must be specified as output before setting this bit. (Reg.0xC8[2]=1)<br>0b: Low<br>1b: High |
| 1 | GPIO1_OUTPUT_DATA | RW | 0 | GPIO1 Output Data<br>The direction of GPIO1 must be specified as output before setting this bit. (Reg.0xC8[1]=1)<br>0b: Low<br>1b: High |
| 0 | GPIO0_OUTPUT_DATA | RW | 0 | GPIO0 Output Data<br>The direction of GPIO1 must be specified as output before setting this bit. (Reg.0xC8[0]=1)<br>0b: Low<br>1b: High |

## 6.78 GPIO Input Data Register (Address = 0xCA)

Table 6-78 GPIO Input Data Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:3 | Reserved | R | 0x00 | Reserved |
| 2 | GPIO2_INPUT_DATA | R | 0 | GPIO2 Input Data<br>The direction of GPIO2 must be specified as input before reading this bit. (Reg.0xC8[2]=0)<br>0b: Low<br>1b: High |
| 1 | GPIO1_INPUT_DATA | R | 0 | GPIO1 Input Data<br>The direction of GPIO1 must be specified as input before reading this bit. (Reg.0xC8[1]=0)<br>0b: Low<br>1b: High |
| 0 | GPIO0_INPUT_DATA | R | 0 | GPIO0 Input Data<br>The direction of GPIO1 must be specified as input before reading this bit. (Reg.0xC8[1]=0)<br>0b: Low<br>1b: High |

## 6.79 Role Judge Finish Register (Address = 0xCB)

Table 6-79 Role Judge Finish Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | Reserved | RW | 00 | Reserved |
| 5 | ROLE_JUDGE_FINISH | RW | 0 | Role Judge Finish:<br>The purpose of this bit is power saving. TCPM should write this bit with a 1b if the role of the device is finished connecting as source/sink. Then, the internal circuit of the device will be activated from power saving mode. However, TCPM should write this bit with a 0b when there is no device connected with the device.<br>0b: The status of the device is power saving mode.<br>1b: The status of the device is activated from power saving mode. |
| 4:0 | Reserved | RW | 0x00 | Reserved |

## 6.80 Over Voltage Detect Register (Address = 0xCC)

Table 6-80 Over Voltage Detect Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | FAULT_PIN_EN | RW | 0 | Fault Pin Enable:<br>The fault pin is assigned to GPIO 2. If TCPM needs to sense the fault event (VBUS OV, DP_DN OV and CC OV), this field must be written with a 1b. In this manner, the device will drive the fault to pin to high when the fault event occurring.<br>1b: Fault pin enable<br>0b: Fault pin disable |
| 6 | DP_DN_OV_SEL | RW | 0 | DP/DN Overvoltage Level Select:<br>The device support two DP/DN overvoltage level. In case DP/DN pin is suffered from abnormal high voltage, the fault pin (GPIO 2) will be drive to high for alerting the TCPM.<br>0b: 4V<br>1b: 4.5V |
| 5 | DP_DN_OV_EN | RW | 0 | DP/DN OV Check Enable<br>0b: No operation<br>1b: Start to check DP/DN overvoltage |
| 4 | VBUS_OV_EN | RW | 0 | VBUS OV Check Enable<br>0b: No operation<br>1b: Start to check VBUS overvoltage |

| | | | | |
|---|---|---|---|---|
| 3:0 | VBUS_OV_SEL | RW | 0x0 | VBUS Overvoltage Select:<br>The VBUS overvoltage can be selected based on the operated VBUS. TCPM could write this field with a 0000b if the VBUS of power stage is operated as 5V. In this manner, when the VBUS is larger than 6V, The device will drive the fault pin (GPIO 2) to high and TCPM will be informed the abnormal situation.<br>0000b: Operated VBUS = 5V, VBUS OV = 6V<br>0001b: Operated VBUS = 6V, VBUS OV = 7.2V<br>0010b: Operated VBUS = 7V, VBUS OV = 8.4V<br>0011b: Operated VBUS = 8V, VBUS OV = 9.6V<br>0100b: Operated VBUS = 9V, VBUS OV = 10.8V<br>0101b: Operated VBUS = 10V, VBUS OV = 12V<br>0110b: Operated VBUS = 11V, VBUS OV = 13.2V<br>0111b: Operated VBUS = 12V, VBUS OV = 14.4V<br>1000b: Operated VBUS = 13V, VBUS OV = 15.6V<br>1001b: Operated VBUS = 14V, VBUS OV = 16.8V<br>1010b: Operated VBUS = 15V, VBUS OV = 18V<br>1011b: Operated VBUS = 16V, VBUS OV = 19.2V<br>1100b: Operated VBUS = 17V, VBUS OV = 20.4V<br>1101b: Operated VBUS = 18V, VBUS OV = 21.6V<br>1110b: Operated VBUS = 19V, VBUS OV = 22.8V<br>1111b: Operated VBUS = 20V, VBUS OV = 24V<br>Note: VBUS OV is set by 1.2 times, compared to the operated VBUS. |

## 6.81 Over Voltage Status Register (Address = 0xCD)

This register is related with Over Voltage Detection Register (Reg.0xCC). Each status bit is effect when Over Voltage Detection Register (Reg.0xCC) is properly set by TCPM.

Table 6-81 Over Voltage Status Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:3 | Reserved | R | 0x00 | Reserved |
| 2 | DP_DN_OV_STATUS | RCU | 0 | DP/DN Overvoltage Status:<br>0b: Cleared<br>1b: DP/DM pin overvoltage level depending on Reg.0xCC [6] |
| 1 | VBUS_OV_STATUS | RCU | 0 | VBUS Overvoltage Status:<br>0b: Cleared<br>1b: VBUS overvoltage level depending on Reg.0xCC [3:0] |
| 0 | CC_OV_STATUS | RCU | 0 | CC Overvoltage Status:<br>The CC pin overvoltage level is fixed to 6.5V. It cannot be set by TCPM.<br>0b: Cleared<br>1b: CC pin overvoltage |

## 6.82 VBUS Control Register (Address = 0xD0)

The FBO pin of UM3500F must be connected to the feedback node of power stage. The upper feedback resistance of power stage needs to select 100k Ohm and the VBUS of power stage also designs to default 5V. Consequently, the VBUS could be increased or decreased by sinking or sourcing current from FBO pin of the UM3500F.

The scale of FBO pin sink/source current is set by 11-bit MCU IT counter (Reg.0xD2~D1). The VBUS is default 5V when MCU IT counter is default C8h (200 in decimal) and the FBO pin is no operation. If the value of MCU IT counter is set to lower than C8h, the FBO pin will source current and the VBUS will be decreased. The lowest VBUS is 3V when MCU IT counter is set to zero. However, in case the value of MCU IT counter is set to larger than C8h (200 in decimal), the FBO pin will sink current and the VBUS will be increased. The highest VBUS is 20.00V when MCU IT counter is 6A4h.

Table 6-82 VBUS Control Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | MCU_CTRL_VOLT_RST | W | 0 | MCU Voltage Control Reset:<br>TCPM reset MCU IT counter and the device will clear this bit automatically.<br>0b: No operation<br>1b: Reset MCU IT counter. VBUS Target Control Register (Reg.0xD1~D2) reset to default value. The VBUS will be reset to 5V when TCPM writes this bit with a 1b |
| 6:1 | Reserved | R | 0x00 | Reserved |

| | | | | |
|---|---|---|---|---|
| 0 | MCU_VOLT _EN_CTRL | RW | 0 | MCU Voltage Control Enable:<br>0b: MCU IT counter is controlled by the device<br>1b: MCU IT counter is controlled by TCPM through setting VBUS Target Control Register (Reg.0xD1~D2) |

## 6.83 VBUS Target Control Byte 0 Register (Address = 0xD1)

Table 6-83 VBUS Target Control Byte 0 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | MCU_IT_CNT_L | RW | 0xC8 | MCU IT Counter Low:<br>The MCU IT counter is validly set only by even number. Each bit of MCU IT counter represents 10mV of VBUS. The resolution of VBUS is 20mV because only even number can be set to MCU IT counter.<br>The MCU IT counter is 11-bit, which is configured as follow equation:<br>MCU_IT_CNT [10:0]= MCU_IT_CNT_H [10:8] + MCU_IT_CNT_L [7:0] |

## 6.84 VBUS Target Control Byte 1 Register (Address = 0xD2)

Table 6-84 VBUS Target Control Byte 1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | MCU _VOLT_SET | RW | 0 | MCU Voltage Set<br>0b: No operation<br>1b: The setting of MCU IT counter is taken effect |
| 6 | Reserved | RW | 0 | Reserved |
| 5 | Reserved | RW | 0 | Reserved |
| 4:3 | Reserved | R | 00 | Reserved |
| 2:0 | MCU_IT_CNT_H | RW | 000 | MCU IT Counter High:<br>The MCU IT counter is validly set only by even number. Each bit of MCU IT counter represents 10mV of VBUS. The resolution of VBUS is 20mV because only even number can be set to MCU IT counter.<br>The MCU IT counter is 11-bit, which is configured as follow equation:<br>MCU_IT_CNT [10:0]= MCU_IT_CNT_H [10:8] + MCU_IT_CNT_L [7:0] |

## 6.85 FW Version High Byte Register (Address = 0xDD)

Table 6-85 FW Version High Byte Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | FW_VER_H | RW | 0x00 | Indicate FW version usage |

## 6.86 FW Version Low Byte Register (Address = 0xDE)

Table 6-86 FW Version Low Byte Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | FW_VER_L | RW | 0x00 | Indicate FW version usage |

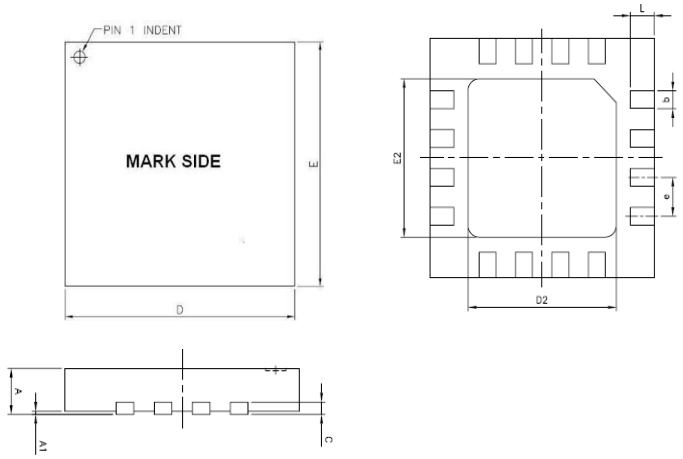
## 6.87 HW Version Register (Address = 0xDF)

Table 6-87 HW Version Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:3 | HW_VER | R | 00001 | HW Ver. |
| 2:0 | Reserved | RW | 000 | Reserved |

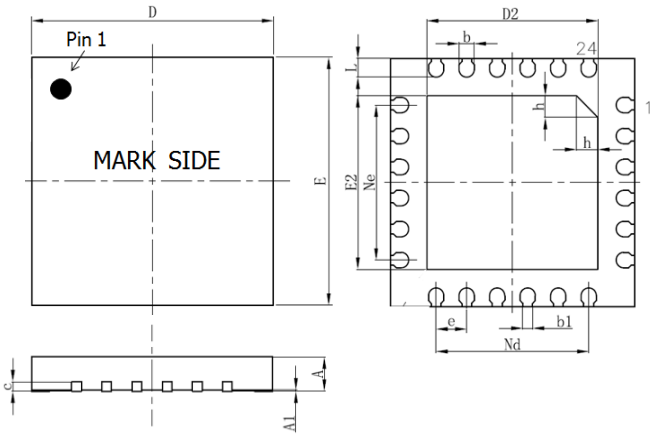
# 7 Package Information

### TQFN-16 4mm × 4mm (pitch 0.65mm) Package (Unit: mm)




| Symbols Unit | Dimension in Millimeter | |
|---|---|---|
| | Min | Max |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| C | 0.18 | 0.30 |
| E | 3.90 | 4.10 |
| D | 3.90 | 4.10 |
| L | 0.45 | 0.65 |
| b | 0.25 | 0.35 |
| e | 0.65 BSC | |
| E2 | 2.00 | 2.30 |
| D2 | 2.00 | 2.30 |

### UTQFN-24L 4mm × 4mm (pitch 0.5mm) Package (Unit: mm)

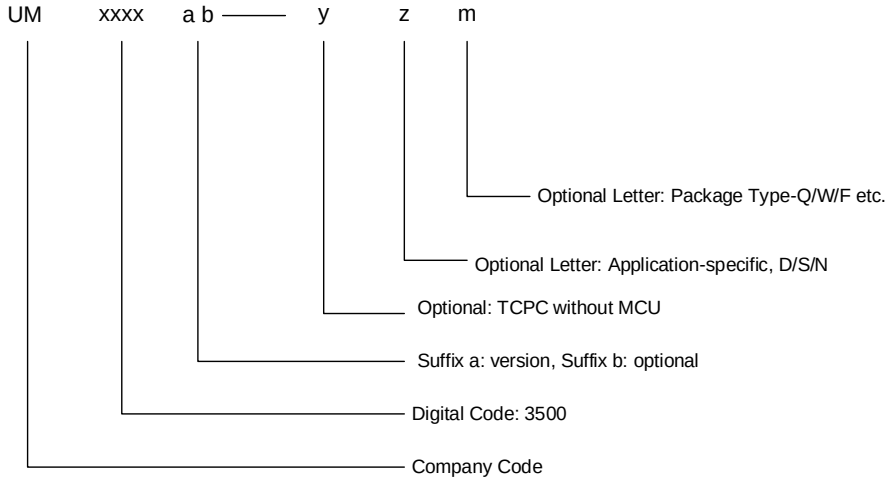



| Symbols Unit | Dimension in Millimeter | |
|---|---|---|
| | Min | Max |
| A | 0.50 | 0.60 |
| A1 | 0.00 | 0.05 |
| C | 0.10 | 0.20 |
| D | 3.90 | 4.10 |
| E | 3.90 | 4.10 |
| b | 0.20 | 0.30 |
| e | 0.50 BSC | |
| Nd | 2.50 BSC | |
| Ne | 2.50 BSC | |
| b1 | 0.16REF | |
| h | 0.30 | 0.40 |
| L | 0.25 | 0.35 |
| D2 | 2.70 | 2.90 |
| E2 | 2.70 | 2.90 |

# 8 Ordering Information

| P/N | Application | Package |
|---|---|---|
| UM3500FA | SRC | UTQFN, 24-Pin |
| UM3500FB | DRP with Dead-battery | TQFN, 16-Pin |
| | | |
| *UM3500FC* | *SRC* | *TQFN, 20-Pin* |
| *UM3500FD* | *DRP with Dead-battery* | *TQFN, 20-Pin* |
| | | |
| | | |
| | | |

Product number code definitions.



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## Revision History

| Revision | Date | Author | Description |
|---|---|---|---|
| V0.1 | 2021/1 | | Initial |
| … | | | |
| … | | | |
| V0.8 | 2022/8 | | 1st Release |
| V0.8a | 2023/10 | | Update version |
| V0.8b | 2023/11 | | Update version |
| | | | |
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